

# **KS8695X**

## **Integrated Multi-Port Gateway Solution**

### **Register Description**

**Version 1.1**  
**January 2008**

**NOTE:**

This information is believed to be accurate and reliable, however no responsibility is assumed by Micrel for its use nor for any infringement of patents or other rights of third parties resulting from its use. No license is granted by implication or otherwise under any patent or patent right of Micrel Inc.

Micrel Confidential

## Table of Contents

<b>1.0 Revision History .....</b>	<b>6</b>
<b>2.0 Memory Map.....</b>	<b>7</b>
<b>3.0 Register Descriptions.....</b>	<b>7</b>
3.1 System Registers .....	7
3.1.1 System Configuration Register (SYSCFG Offset 0x0000) .....	7
3.1.2 System Clock and Bus Control Register (CLKCON Offset 0x0004).....	8
3.2 Memory Controller Register.....	9
3.2.1 External I/O Access Control Register 0(EXTACON0 Offset 0x4000) .....	9
3.2.2 External I/O Access Control Register 1(EXTACON1 Offset 0x4004) .....	9
3.2.3 External I/O Access Control Register 2(EXTACON2 Offset 0x4008) .....	12
3.2.4 ROM/SRAM/FLASH Control Register 0(ROMCON0 Offset 0x4010).....	13
3.2.5 ROM/SRAM/FLASH Control Register 1(ROMCON1 Offset 0x4014).....	14
3.2.6 External I/O and ROM/SRAM/FLASH General Register (ERGCON Offset 0x4020).....	15
3.2.7 SDRAM Control Register 0(SDCON0 Offset 0x4030).....	16
3.2.8 SDRAM Control Register 1(SDCON1 Offset 0x4034).....	16
3.2.9 SDRAM General Control Register (SDGCON Offset 0x4038).....	17
3.2.10 SDRAM Buffer Control Register (SDBCON Offset 0x403C).....	17
3.2.11 SDRAM Refresh Timer Register (REFTIM Offset 0x4040).....	18
3.3 WAN DMA Registers .....	19
3.3.1 WAN MAC DMA Transmit Control Register (WMDTXC Offset 0x6000).....	19
3.3.2 WAN MAC DMA Receive Control Register (WMDRXC Offset 0x6004) .....	20
3.3.3 WAN MAC DMA Transmit Start Command Register (WMDTSC Offset 0x6008).....	21
3.3.4 WAN MAC DMA Receive Start Command Register (WMDRSC Offset 0x600C).....	21
3.3.5 WAN Transmit Descriptor List Base Address Register (WTDLB Offset 0x6010).....	21
3.3.6 WAN Receive Descriptor List Base Address Register (WRDLB Offset 0x6014) .....	22
3.3.7 WAN MAC Station Address Low Register (WMAL Offset 0x6018).....	22
3.3.8 WAN MAC Station Address High Register (WMAH Offset 0x601C).....	22
3.3.9 WAN MAC Additional Station Address Low Register (WMAAL0-15) .....	23
3.3.10 WAN MAC Additional Station Address High Register (WMAAH0-15).....	23
3.4 LAN DMA Registers.....	24
3.4.1 LAN MAC DMA Transmit Control Register (LMDTXC Offset 0x8000).....	24
3.4.2 LAN MAC DMA Receive Control Register (LMDRXC Offset 0x8004).....	25
3.4.3 LAN MAC DMA Transmit Start Command Register (LMDTSC Offset 0x8008) .....	27
3.4.4 LAN MAC DMA Receive Start Command Register (LMDRSC Offset 0x800C) .....	27
3.4.5 LAN Transmit Descriptor List Base Address Register (LTDLB Offset 0x8010) .....	27
3.4.6 LAN Receive Descriptor List Base Address Register (LRDLB Offset 0x8014).....	28
3.4.7 LAN MAC Station Address Low Register (LMAL Offset 0x8018) .....	28
3.4.8 LAN MAC Station Address High Register (LMAH Offset 0x801C).....	28
3.4.9 LAN MAC Additional Station Address Low Register (LMAAL0-15) .....	28
3.4.10 LAN MAC Additional Station Address High Register (LMAAH0-15).....	29
3.5 UART Registers .....	30
3.5.1 UART Receive Buffer Register (URRB Offset 0xE000) .....	30
3.5.2 UART Transmit Holding Register (URTH Offset 0xE004).....	30
3.5.3 UART FIFO Control Register (URFC Offset 0xE008).....	31
3.5.4 UART Line Control Register (URLC Offset 0xE00C) .....	31

3.5.5	UART Modem Control Register (URMC Offset 0xE010).....	33
3.5.6	UART Line Status Register (URLS Offset 0xE014).....	33
3.5.7	UART Modem Status Register (URMS Offset 0xE018).....	35
3.5.8	UART Baud Rate Divisor Register (URBD Offset 0xE01C).....	35
3.5.9	UART Status Register (USR Offset 0xE020).....	36
3.6	Interrupt Controller Registers.....	36
3.6.1	Interrupt Mode Control Register (INTMC Offset 0xE200).....	36
3.6.2	Interrupt Enable Register (INTEN Offset 0xE204).....	39
3.6.3	Interrupt Status Register (INTST Offset 0xE208).....	41
3.6.4	Interrupt Priority Register for WAN MAC (INTPW Offset 0xE20C).....	43
3.6.5	Interrupt Priority Register for LAN MAC (INTPL Offset 0xE214).....	44
3.6.6	Interrupt Priority Register for Timer (INTPT Offset 0xE218).....	44
3.6.7	Interrupt Priority Register for UART (INTPU Offset 0xE21C).....	45
3.6.8	Interrupt Priority Register for External Interrupt (INTPE Offset 0xE220).....	45
3.6.9	Interrupt Priority Register for Communications Channel (INTPC Offset 0xE224).....	46
3.6.10	Interrupt Priority Register for Bus Error Response (INTPBE Offset 0xE228).....	46
3.6.11	Interrupt Mask Status Register (INTMS Offset 0xE22C).....	46
3.6.12	Interrupt Pending Highest Priority Register for PIO (INTHPF Offset 0xE230).....	48
3.6.13	Interrupt Pending Highest Priority Register for IRQ (INTHPI Offset 0xE234).....	50
3.7	Timer Registers.....	52
3.7.1	Timer Control Register (TMCON Offset 0xE400).....	52
3.7.2	Timer 1 Timeout Count Register (T1TC Offset 0xE404).....	53
3.7.3	Timer 0 Timeout Count Register (T0TC Offset 0xE408).....	53
3.7.4	Timer 1 Pulse Count Register (T1PD Offset 0xE40C).....	53
3.7.5	Timer 0 Pulse Count Register (T0PD Offset 0xE410).....	54
3.8	GPIO Registers.....	54
3.8.1	I/O Port Mode Register (IOPM Offset 0xE600).....	54
3.8.2	I/O Port Control Register (IOPC Offset 0xE604).....	55
3.8.3	I/O Port Data Register (IOPD Offset 0xE608).....	56
3.9	Switch Engine Registers.....	56
3.9.1	Switch Engine Control 0 Register (SEC0 Offset 0xE800).....	57
3.9.2	Switch Engine Control 1 Register (SEC1 Offset 0xE804).....	58
3.9.3	Port 1 Configuration Register (SEP1C Offset 0xE808).....	58
3.9.4	Port 2 Configuration Register (SEP2C Offset 0xE80C).....	59
3.9.5	Port 3 Configuration Register (SEP3C Offset 0xE810).....	59
3.9.6	Port 4 Configuration Register (SEP4C Offset 0xE814).....	60
3.9.7	Port 5 Configuration Register (SEP5C Offset 0xE818).....	60
3.9.8	Ports 1 & 2 Auto Negotiation (AN) Register (SEP12AN Offset 0xE81C).....	60
3.9.9	Ports 3 & 4 Auto Negotiation (AN) Register (SEP34AN Offset 0xE820).....	61
3.9.10	Look-up Engine (LUE) Control Register (SELUEC Offset 0xE824).....	62
3.9.11	Look-up Engine (LUE) Indirect Register High (SELUEIH Offset 0xE828).....	63
3.9.12	Look-up Engine (LUE) Indirect Register Low (SELUEIL Offset 0xE82C).....	63
3.9.13	Advance Feature Control Register (SEAFEC Offset 0xE830).....	64
3.9.14	DSCP Register High (SEDSCPH Offset 0xE834).....	65
3.9.15	DSCP Register Low (SEDSCPL Offset 0xE838).....	65
3.9.16	Switch Engine MAC Address Register High (SEMAH Offset 0xE83C).....	65

3.9.17	Switch Engine MAC Address Register Low (SEMAL Offset 0xE840) .....	65
3.9.18	Management Counter Indirect Access Register (SEMCIA Offset 0xE844) .....	66
3.9.19	Management Counter Data Register (SEMCD Offset 0xE848).....	66
3.9.20	LAN PHY Power Management Register for Ports 1 & 2 (LPPM12 Offset 0xE84C).....	68
3.9.21	LAN PHY Power Management Register for Ports 3 & 4 (LPPM34 Offset 0xE850) .....	69
3.10	Miscellaneous Registers .....	70
3.10.1	Device ID Register (DID Offset 0xEA00).....	70
3.10.2	Revision ID Register (RID Offset 0xEA04) .....	71
3.10.3	WAN Miscellaneous Control Register (WMC Offset 0xEA0C) .....	71
3.10.4	WAN PHY Power Management Register (WPPM Offset 0xEA10) .....	72
3.10.5	Test Register 1(WPC Offset 0xEA14).....	73
3.10.6	Test Register 2 (WPS Offset 0xEA18) .....	73
<b>4.0</b>	<b>Host Communication.....</b>	<b>73</b>
4.1	Descriptor Lists and Data buffers .....	73
4.2	Receive Descriptors (RDES0-RDES3) .....	74
4.3	Transmit Descriptors (TDES0-TDES3) .....	76

## 1.0 Revision History

Revision	Date	Name	Description
1.0	1-16-04	R. Yeh	First Release
1.1	1-03-08	A. Duvall	Add note to Register RDES0[23:20] and TDES1[23:20]. Reformatted document.

Micrel Confidential

## 2.0 Memory Map

Upon power up, the KS8695X memory map is configured as shown below.

Address Range	Region Size	Description
0x03FF0000-0x04000000	64 kbytes	KS8695X System Configuration Register Space
0x02000000-0x03FEFFFF	32Mbytes	Not Configured
0x00000000-0x01FFFFFF	32 Mbytes	Flash Bank 0

The default base address for the the KS8695X system configuration registers is 0x03ff0000. After power up, the user is free to remap the memory for his/her specific application. Here is an example of the memory space remapped for operation:

Address Range	Region Size	Description
0x03FF0000-0x04000000	64 kbyte	KS8695X System Configuration Register Space
0x02900000-0x03FEFFFF	23 Mbyte	Spare (External I/O)
0x02100000-0x028FFFFF	8 Mbyte	FLASH
0x00100000-0x020FFFFF	32 Mbyte	SDRAM
0x00000000-0x0007FFFF	512 kbyte	SRAM

## 3.0 Register Descriptions

The KS8695X registers are grouped as follows in the 64kbyte System Configuration Register space.

Address Range	Description
0x0000 – 0x0004	System Registers
0x4000 – 0x4040	Memory Controller Interface Registers
0x6000 – 0x60FC	WAN DMA Registers
0x8000 – 0x80FC	LAN DMA Registers
0xE000 – 0xE020	UART Registers
0xE200 – 0xE230	Interrupt Controller Registers
0xE400 – 0xE410	Timer Registers
0xE600 – 0xE608	General Purpose I/O Registers
0xE800 – 0xE850	Switch Engine Configuration Registers
0xEA00- 0xEA18	Miscellaneous Registers

The following is a detailed list of register bit descriptions. It is meant to be used as a reference for development.

### 3.1 System Registers

#### 3.1.1 System Configuration Register (SYSCFG Offset 0x0000)

The register determines the start address of all the system control registers. The total system control register space is fixed at 64Kbytes boundary.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	0H	RO	Reserved
25:16	3FFH	RW	SPRBP System Configuration Register Bank Base Pointer The Base address of the system configuration register bank. The resolution of the address is 64Kbytes. Note: to place the start address at 1800000H, use the formula: setting value = ( 1800000H / 64K ) << 16.
15:0	0	RO	Reserved

### 3.1.2 System Clock and Bus Control Register (CLKCON Offset 0x0004)

The CLKCON register is written by the CPU to control the internal clock divider for the system clock.

The following table shows the CLKCON register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION																							
31:9	0		Reserved																							
8	0	RW	SFMODE System Fast Mode for Simulation This bit is for simulation only. Software should never set this bit.																							
7:3	0	RO	Reserved																							
2:0	111b	RW	SCDC System Clock Divider Select The internal system clock source is derived from the levels at the CLKSEL and SCLK pins. If CLKSEL is Low, the internal system clock source is the XCLK1 pin. If CLKSEL is High, the internal system clock source is the internal PLL clock synthesizer (5x of XCLK1). The internal system clock is divided by this value. The divided clock is then used to drive the CPU and system peripherals.If all bits are zero, a non-divided clock is used. The system/CPU clock is selected according to the following table:																							
			<table><tr><th></th><th>System Clock</th><th>CPU Clock</th></tr><tr><td>000</td><td>125 MHz</td><td rowspan="2">166 MHz</td></tr><tr><td>001</td><td>100 MHz</td></tr><tr><td>010</td><td>62.5 MHz</td><td rowspan="2">83 MHz</td></tr><tr><td>011</td><td>50 MHz</td></tr><tr><td>100</td><td>41.7 MHz</td><td rowspan="2">55.3 MHz</td></tr><tr><td>101</td><td>33.3 MHz</td></tr><tr><td>110</td><td>31.3 MHz</td><td rowspan="2">41.5 MHz</td></tr><tr><td>111</td><td>25 MHz</td></tr></table>		System Clock	CPU Clock	000	125 MHz	166 MHz	001	100 MHz	010	62.5 MHz	83 MHz	011	50 MHz	100	41.7 MHz	55.3 MHz	101	33.3 MHz	110	31.3 MHz	41.5 MHz	111	25 MHz
	System Clock	CPU Clock																								
000	125 MHz	166 MHz																								
001	100 MHz																									
010	62.5 MHz	83 MHz																								
011	50 MHz																									
100	41.7 MHz	55.3 MHz																								
101	33.3 MHz																									
110	31.3 MHz	41.5 MHz																								
111	25 MHz																									



## 3.2 Memory Controller Register

### 3.2.1 External I/O Access Control Register 0(EXTACON0 Offset 0x4000)

The system has three external I/O access control registers that control external I/O banks. These registers correspond to the three external I/O banks that are supported by the KS8695.

External I/O access cycles are controlled through these registers (EXTACON0, EXTACON1, EXTACON2), or through an external wait signals, EWAITN. The delay times of the control signals (OEN, WBEN, ECSN) can be programmed to obtain access cycles that are longer than those possible with a specified value.

The following table shows the EXTACON0 register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EBONPTR External I/O Bank 0 Last Address Pointer This value is the current bank end address. The last address is calculated as {EBONPTR, 0xffff}.
21:12	-	RW	EBOBPTR External I/O Bank 0 Base Pointer This value is the start address of the External I/O Bank 1. The start address is calculated as EBOBPTR << 16.
11:9	-	RW	EBOTACT External I/O Bank 0 Write Enable/Output Enable Active Time The access time for Bank 0 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles Note: Please see section 3.2.6 for TMULT definition.
8:6	-	RW	EBOTCON External I/O Bank 0 Chip Select Hold Time The Chip Select Hold time for Bank 0 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
5:3	-	RW	EBOTACS External I/O Bank 0 Address Setup Time before ECSN The address setup time for Bank 0 is defined in unit of system clock. 000 = 0 cycle 001 = TMULT + 1 cycles 010 = 2 x TMULT + 2 cycles 011 = 3 x TMULT + 3 cycles 100 = 4 x TMULT + 4 cycles 101 = 5 x TMULT + 5 cycles 110 = 6 x TMULT + 6 cycles

			111 = 7 x TMULT + 7 cycles
2:0	-	RW	EB0TCOS External I/O Bank 0 Chip Select Setup Time before OEN The chip select setup time for Bank 0 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles

### 3.2.2 External I/O Access Control Register 1(EXTACON1 Offset 0x4004)

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EB1NPTR External I/O Bank 1 Last Address Pointer This value is the current bank end address. The last address is calculated as {EB1NPTR, 0xffff}.
21:12	-	RW	EB1BPTR External I/O Bank 1 Base Pointer This value is the start address of the External I/O Bank 1. The start address is calculated as EB1BPTR << 16.
11:9	-	RW	EB1TACT External I/O Bank 1 Write Enable/Output Enable Active Time The access time for Bank 1 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
8:6	-	RW	EB1TCOH External I/O Bank 1 Chip Select Hold Time The Chip Select Hold time for Bank 1 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
5:3	-	RW	EB1TACS External I/O Bank 1 Address Setup Time before ECSN The address setup time for Bank 1 is defined in unit of system clock. 000 = 0 cycle 001 = TMULT + 1 cycles 010 = 2 x TMULT + 2 cycles

			011 = 3 x TMULT + 3 cycles 100 = 4 x TMULT + 4 cycles 101 = 5 x TMULT + 5 cycles 110 = 6 x TMULT + 6 cycles 111 = 7 x TMULT + 7 cycles
2:0	-	RW	EB1TCOS External I/O Bank 1 Chip Select Setup Time before OEN The chip select setup time for Bank 1 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles

### 3.2.3 External I/O Access Control Register 2(EXTACON2 Offset 0x4008)

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	EB2NPTR External I/O Bank 2 Last Address Pointer This value is the current bank end address. The last address is calculated as {EB2NPTR, 0xffff}.
21:12	-	RW	EB2BPTR External I/O Bank 2 Base Pointer This value is the start address of the External I/O Bank 2. The start address is calculated as EB2BPTR << 16.
11:9	-	RW	EB2TACT External I/O Bank 2 Write Enable/Output Enable Active Time The access time for Bank 2 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
8:6	-	RW	EB2TCOH External I/O Bank 2 Chip Select Hold Time The Chip Select Hold time for Bank 2 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles 110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
5:3	-	RW	EB2TACS External I/O Bank 2 Address Setup Time before ECSN The address setup time for Bank 2 is defined in unit of system clock. 000 = 0 cycle 001 = TMULT + 1 cycles 010 = 2 x TMULT + 2 cycles 011 = 3 x TMULT + 3 cycles 100 = 4 x TMULT + 4 cycles 101 = 5 x TMULT + 5 cycles 110 = 6 x TMULT + 6 cycles 111 = 7 x TMULT + 7 cycles
2:0	-	RW	EB2TCOS External I/O Bank 2 Chip Select Setup Time before OEN The chip select setup time for Bank 2 is defined in unit of system clock. 000 = 1 cycle 001 = TMULT + 2 cycles 010 = 2 x TMULT + 3 cycles 011 = 3 x TMULT + 4 cycles 100 = 4 x TMULT + 5 cycles 101 = 5 x TMULT + 6 cycles

			110 = 6 x TMULT + 7 cycles 111 = 7 x TMULT + 8 cycles
--	--	--	--

### 3.2.4 ROM/SRAM/FLASH Control Register 0 (ROMCON0 Offset 0x4010)

The KS8695X has two control registers for ROM, SRAM, and FLASH memory. These registers correspond to the two ROM/SRAM/FLASH banks that are supported by the KS8695.

For ROM/SRAM/FLASH bank 0, the external data bus width is determined by the B0SIZE[1:0] pins.

When B0SIZE[1:0] = "01", the external bus width for ROM/SRAM/FLASH bank 0 is 8 bits.

When B0SIZE[1:0] = "10", the external bus width for ROM/SRAM/FLASH bank 0 is 16 bits.

When B0SIZE[1:0] = "11", the external bus width for ROM/SRAM/FLASH bank 0 is 32 bits.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	1FFH	RW	RBONPTR ROM/SRAM/FLASH Bank 0 Next Pointer This value is the current bank end address. The last address is calculated as {RBONPTR, 0xffff}.
21:12	0	RW	RB0BPTR ROM/SRAM/FLASH Bank 0 Base Pointer This value is the start address of the ROM/SRAM/FLASH Bank 0. The start address is calculated as RB0BPTR << 16.
11:7	0	RO	Reserved
6:4	111B	RW	RB0TACC ROM/SRAM/FLASH Bank 0 Access Cycle Time The access cycle time is defined in unit of system clock. Note that the write cycle access time is at least 3 cycles. 000 = 3 cycles if TMULT = 0 for write cycles 000 = TMULT + 2 cycles if TMULT > 0 for write cycles 000 = TMULT + 2 cycles for read cycles 001 = 2 x TMULT + 3 cycles 010 = 3 x TMULT + 4 cycles 011 = 4 x TMULT + 5 cycles 100 = 5 x TMULT + 6 cycles 101 = 6 x TMULT + 7 cycles 110 = 7 x TMULT + 8 cycles 111 = 8 x TMULT + 9 cycles
3:2	11B	RW	RB0TPA ROM/SRAM/FLASH Bank 0 Page Address Access Time The access cycle time is specified in unit of system clock. 00 = TMULT + 2 cycles 01 = 2 x TMULT + 3 cycles 10 = 3 x TMULT + 4 cycles 11 = 4 x TMULT + 5 cycles
1:0	0	RW	RB0PMC ROM/SRAM/FLASH Bank 0 Page Mode Configuration The RB0PMC configures the access size in page mode. 00 = Normal ROM 01 = 4-word page 10 = 8 word page 11 = 16 word page

### 3.2.5 ROM/SRAM/FLASH Control Register 1(ROMCON1 Offset 0x4014)

The KS8695X has two control registers for ROM, SRAM, and FLASH memory. These registers correspond to the two ROM/SRAM/FLASH banks that are supported by the KS8695.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	RB1NPTR ROM/SRAM/FLASH Bank 1 Next Pointer This value is the current bank end address. The last address is calculated as {RB1NPTR, 0xffff}.
21:12	-	RW	RB1BPTR ROM/SRAM/FLASH Bank 1 Base Pointer This value is the start address of the ROM/SRAM/FLASH Bank 1. The start address is calculated as RB1BPTR << 16.
11:7	0	RO	Reserved
6:4	-	RW	RB1TACC ROM/SRAM/FLASH Bank 1 Access Cycle Time The access cycle time is defined in unit of system clock. Note that the write cycle access time is at least 3 cycles. 000 = 3 cycles if TMULT = 0 for write cycles 000 = TMULT + 2 cycles if TMULT > 0 for write cycles 000 = TMULT + 2 cycles for read cycles 001 = 2 x TMULT + 3 cycles 010 = 3 x TMULT + 4 cycles 011 = 4 x TMULT + 5 cycles 100 = 5 x TMULT + 6 cycles 101 = 6 x TMULT + 7 cycles 110 = 7 x TMULT + 8 cycles 111 = 8 x TMULT + 9 cycles
3:2	-	RW	RB1TPA ROM/SRAM/FLASH Bank 1 Page Address Access Time The access cycle time is specified in unit of system clock. 00 = TMULT + 2 cycles 01 = 2 x TMULT + 3 cycles 10 = 3 x TMULT + 4 cycles 11 = 4 x TMULT + 5 cycles
1:0	-	RW	RB1PMC ROM/SRAM/FLASH Bank 1 Page Mode Configuration The RB1PMC configures the access size in page mode. 00 = Normal ROM 01 = 4-word page 10 = 8 word page 11 = 16 word page

### 3.2.6 External I/O and ROM/SRAM/FLASH General Register (ERGCON Offset 0x4020)

The KS8695X supports 8/16/32-bit external ROM/SRAM/FLASH memory and I/O interfaces. By programming this register, the data width of the ROM/SRAM/FLASH memory and I/O interfaces can be controlled.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	0	RO	Reserved
29:28	3H	RW	TMULT External I/O and ROM/SRAM/FLASH Time Multiplier 00 = Multiply by 0 01 = Multiply by 1 10 = Multiply by 2 11 = Multiply by 3
27:24	0	RO	Reserved
23:22	0	RW	Reserved
21:20	0	RW	DSX2 Data Width for External I/O Bank 2 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
19:18	0	RW	DSX1 Data Width for External I/O Bank 1 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
17:16	0	RW	DSX0 Data Width for External I/O Bank 0 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
15:8	0	RO	Reserved
7:6	0	RW	Reserved
5:4	0	RW	Reserved
3:2	0	RW	DSR1 Data Width for ROM/SRAM/FLASH Bank 1 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)
1:0	-	RW	DSR0 Data Width for ROM/SRAM/FLASH Bank 0 00 = disabled 01 = Byte ( 8 bits ) 10 = Half-word (16 bits) 11 = Word (32 bits)  Note: DSR0's value is derived from B0SIZE[1:0] upon power on reset. After power on reset, it can be written with 00B to disable the bank or the value of B0SIZE[1:0] to enable the bank. Any other written values are ignored.

### 3.2.7 SDRAM Control Register 0(SDCON0 Offset 0x4030)

The KS8695X has two control registers for SDRAM memory. These registers correspond to the two SDRAM banks that are supported by the KS8695.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	DB0NPTR SDRAM Bank 0 Last Address Pointer This value is the current bank end address. The last address is calculated as {DB0NPTR, 0xffff}.
21:12	-	RW	DB0BPTR SDRAM Bank 0 Base Pointer This value is the start address of the SDRAM Bank 0. The start address is calculated as DB0BPTR << 16.
11:10	0	RO	Reserved
9:8	-	RW	DB0CAB SDRAM Bank 0 Column Address Bits This field selects the number of column address bits for the SDRAM. 00 = 8 bits 01 = 9 bits 10 = 10 bits 11 = 11 bits
7:4	0	RO	Reserved
3	-	RW	DB0BNUM SDRAM Bank 0 Number of Banks 0 = 2 Bank Device 1 = 4 Bank Device
2:1	0	RW	DB0DBW SDRAM Bank 0 Data Bus Width 00 = Disabled 01 = 8 Bit 10 = 16 Bits 11 = 32 Bits
0	0	RO	Reserved

### 3.2.8 SDRAM Control Register 1(SDCON1 Offset 0x4034)

The KS8695X has two control registers for SDRAM memory. These registers correspond to the two SDRAM banks that are supported by the KS8695.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:22	-	RW	DB1NPTR SDRAM Bank 1 Last Address Pointer This value is the current bank end address. The last address is calculated as {DB1NPTR, 0xffff}.
21:12	-	RW	DB1BPTR SDRAM Bank 1 Base Pointer This value is the start address of the SDRAM Bank 1. The start address is calculated as DB1BPTR << 16.
11:10	0	RO	Reserved
9:8	-	RW	DB1CAB SDRAM Bank 1 Column Address Bits



			This field selects the number of column address bits for the SDRAM. 00 = 8 bits 01 = 9 bits 10 = 10 bits 11 = 11 bits
7:4	0	RO	Reserved
3	-	RW	DB1BNUM SDRAM Bank 1 Number of Banks 0 = 2 Bank Device 1 = 4 Bank Device
2:1	0	RW	DB1DBW SDRAM Bank 1 Data Bus Width 00 = Disabled 01 = 8 Bit 10 = 16 Bits 11 = 32 Bits
0	0	RO	Reserved

### 3.2.9 SDRAM General Control Register (SDGCON Offset 0x4038)

This register controls the global setting of the SDRAM controller.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:9	0	RO	Reserved
8	0	RW	Reserved
7:4	0	RO	Reserved
3:2	-	RW	SDTRC SDRAM RAS to CAS Latency 00 = 1 Cycle 01 = 2 Cycles 10 = 3 Cycles 11 = 4 Cycles
1:0	-	RW	SDCAS SDRAM CAS Latency 00 = 1 Cycle 01 = 2 Cycles 10 = 3 Cycles 11 = 4 Cycles

### 3.2.10 SDRAM Buffer Control Register (SDBCON Offset 0x403C)

This register configures the function of the read and write buffer in the memory controller.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	SDESTA SDRAM Engine Status Bit 0 = SDRAM engine is idle.

			1 = SDRAM engine is busy.
30:24	0	RO	Reserved
24	0	RW	RBUFBDIS Read Buffer Burst Enable. This bit controls the read burst length for on-chip AMBA bus incremental burst when RBUFEN is reset. This bit is ignored when RBUFEN is set. 0 = Read buffer burst is disabled for the incremental burst. 1 = Read buffer burst is enabled for the incremental burst.
23	0	RW	WFIFOEN Write FIFO Enable. 0 = Write FIFO is disabled. 1 = Write FIFO is enabled.
22	0	RW	RBUFEN Read Buffer Enable. 0 = Read buffer is disabled. 1 = Read buffer is enabled.
21	0	RW	FLUSHWFIFO Flush Write FIFO Writing a "1" to this bit causes the write FIFO to be flushed to the SDRAM memory. After the flush, this bit is cleared.
20	0	RW	RBUFINV Read Buffer Invalidate Writing a "1" to this bit invalidates the read buffer. After the invalidation, this bit is cleared.
19:18	0	RO	Reserved
17:16	0	RW	SDINI SDRAM Initialization Control After the command is issued, SDINI is reset. 00 = Normal Operation. 01 = Issue a Precharge All Banks Command to the SDRAM. 10 = Issue a Mode Command to the SDRAM. 11 = Issue a NOP to the SDRAM.
15:14	0	RO	Reserved
13:0	-	RW	SDMODE SDRAM Mode Register Program Value During the issue of mode command to the SDRAM, SDMODE[13:0] also goes out to ADDR[13:0].

### 3.2.11 SDRAM Refresh Timer Register (REFTIM Offset 0x4040)

The refresh timer register is a 16-bit read/write register that is programmed with the number of network clocks (XCLK1) ticks that should be counted between SDRAM refresh cycles.

For example, for the common refresh period of 16 $\mu$ s, and a network clock frequency of 25MHz, the following value should be programmed into it:

$$16 \times 10^{-6} \times 25 \times 10^6 = 400$$

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0	RO	Reserved
15:0	0	RW	REFTIM Refresh Timer Value A value of 0 disables refresh timer.

### 3.3 WAN DMA Registers

#### 3.3.1 WAN MAC DMA Transmit Control Register (WMDTXC Offset 0x6000)

The WAN MAC DMA transmit control register establishes the transmit operating modes and commands for the WAN port. This register should be one of the last SCRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	WO	WMTRST WAN DMA Soft Reset When set, the WAN MAC DMA block is reset. All registers in the WAN MAC DMA block will be reset to the default values.
30		RO	Reserved
29:24	0	RW	WMTBS WAN DMA Transmit Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the WAN MAC DMA burst size is limited only by the amount of data stored in the transmit buffer before issuing a bus request. The WMTBS can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the WMTBS default is 0, i.e. unlimited.
23:19	0	RO	Reserved
18	0	RW	WMTUCG WAN MAC Transmit UDP Checksum Generate When set, the KS8695X will generate correct UDP checksum for outgoing UDP/IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
17	0	RW	WMTTCG WAN MAC Transmit TCP Checksum Generate When set, the KS8695X will generate correct TCP checksum for outgoing TCP/IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
16	0	RW	WMTICG WAN MAC Transmit IP Checksum Generate When set, the KS8695X will generate correct IP checksum for outgoing IP frames at WAN port. When this bit is set, ADD CRC should also turn on.
15:10	0	RO	Reserved
9	0	RW	WMTFCE WAN MAC Transmit Flow Control Enable When this bit is set and the KS8695X is in Full Duplex mode, flow control is enabled and the KS8695X will transmit a PAUSE frame when the MAC DMA Receive Buffer capacity has reached a level that may cause the buffer to overflow. When this bit is set and the KS8695X is in Half Duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
8	0	RW	WMTLB WAN MAC DMA Loop Back Mode Select the KS8695X WAN port in loopback operation modes. When set, the packet to be sent will be returned at the MAC interface.
7:3	0	RO	Reserved
2	0	RW	WMTEP WAN MAC DMA Transmit Enable Padding When set, the KS8695X automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	RW	WMTAC WAN MAC DMA Transmit Add CRC

			When set, the KS8695X appends the CRC to the end of the transmission frame.
0	0	RW	<b>WMTE WAN MAC DMA TX Enable</b> When the bit is set, the MDMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

## 3.3.2 WAN MAC DMA Receive Control Register (WMDRXC Offset 0x6004)

The WAN MAC DMA receive control register establishes the receive operating modes and commands for the WAN port. This register should be one of the last SCRs to be written as part of the receive initialization.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	0	RO	Reserved
29:24	0	RW	<b>WMRBS WAN DMA Receive Burst Size</b> This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the WAN MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The WMRBS can be programmed with permissible values 0, 1, 2, 4, 8, 16, or 32. After reset, the WMRBS default is 0, i.e. unlimited.
23:19	0	RO	Reserved
18	0	RW	<b>WMRUCC WAN MAC Receive UDP Checksum Check</b> When set, the KS8695X will check for correct UDP checksum for incoming UDP/IP frames at WAN port. Packets received with incorrect UDP checksum will be discarded.
17	0	RW	<b>WMRTCC WAN MAC Receive TCP Checksum Check</b> When set, the KS8695X will check for correct TCP checksum for incoming TCP/IP frames at WAN port. Packets received with incorrect TCP checksum will be discarded.
16	0	RW	<b>WMRICC WAN MAC Receive IP Checksum Check</b> When set, the KS8695X will check for correct IP checksum for incoming IP frames at WAN port. Packets received with incorrect IP checksum will be discarded.
15:10	0	RO	Reserved
9	0	RW	<b>WMRFCE WAN MAC Receive Flow Control Enable</b> When this bit is set and the KS8695X is in Full Duplex mode, flow control is enabled and the KS8695X will acknowledge a PAUSE frame from the WAN port, i.e. the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, no flow control is enabled.
8:7	0	RO	Reserved
6	0	RW	<b>WMRB WAN MAC Receive Broadcast</b> When set, the WAN MAC receive all broadcast frames.
5	0	RW	<b>WMRM WAN MAC Receive Multicast</b> When set, the WAN MAC receive all multicast frames (including broadcast).
4	0	RW	<b>WMRU WAN MAC Receive Unicast</b> When set, the WAN MAC receive unicast frames that match the 48-bit Station Address of the WAN MAC.
3	0	RW	<b>WMRE WAN MAC DMA Receive Error Frame</b>

			When set, the KS8695X will pass the errors frames received to the host. Error frames include runt frames, oversized frames, CRC errors.
2	0	RW	WMRA WAN MAC DMA Receive All When set, the KS8695X receives all incoming frames, regardless of its destination address.
1	0	RO	Reserved
0	0	RW	WMRE WAN MAC DMA RX Enable When the bit is set, the DMA RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.

### 3.3.3 WAN MAC DMA Transmit Start Command Register (WMDTSC Offset 0x6008)

This register is written by the the CPU when packets in the WAN data buffer need to be transmitted.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0	WO	WTSC WAN Transmit Start Command When written with any value, the WAN Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptors are available, the transmit process starts or resumes. This bit is self-clearing.

### 3.3.4 WAN MAC DMA Receive Start Command Register (WMDRSC Offset 0x600C)

This register is written by the the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0	WO	WRSC WAN Receive Start Command When written with any value, the WAN Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and wait for the next receive restart command. If descriptors are available, the receive process resumes. This bit is self-clearing.

### 3.3.5 WAN Transmit Descriptor List Base Address Register (WTDLB Offset 0x6010)

This register is used for WAN Transmit descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695X behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31:2	0	RW	WSTL WAN Start of Transmit List Note: Write can only occur when the transmit process stopped.
1:0	0	RO	Reserved

### 3.3.6 WAN Receive Descriptor List Base Address Register (WRDLB Offset 0x6014)

This register is used for WAN Receive descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.  
Note: The descriptor lists must be Word (32-bit) aligned. The KS8695X behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31:2	0	RW	WSRL WAN Start of Receive List Note: Write can only occur when the transmit process stopped.
1:0	0	RO	Reserved

### 3.3.7 WAN MAC Station Address Low Register (WMAL Offset 0x6018)

Station Address is used to define the individual destination address the KS8695X WAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31:0	0	RW	WMAL WAN MAC Station Address Low 4 bytes The least significant word of the WAN MAC station address.

### 3.3.8 WAN MAC Station Address High Register (WMAH Offset 0x601C)

Station Address is used to define the individual destination address the KS8695X WAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.



The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31:16	0	RO	Reserved
15:0	0	RW	WMAL WAN MAC Station Address High 2 bytes The most significant word of the WAN MAC station address.

### 3.3.9 WAN MAC Additional Station Address Low Register (WMAAL0-15)

The KS8695X supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695X will respond to when receiving frames on the WAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31:0	--	RW	WMAAL0 WAN MAC Additional Station Address 0 Low 4 bytes The least significant word of the additional WAN MAC 0 station address.

### 3.3.10 WAN MAC Additional Station Address High Register (WMAAH0-15)

The KS8695X supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695X will respond to when receiving frames on the WAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

<b>BIT FIELD</b>	<b>DEFAULT VALUE</b>	<b>READ/ WRITE</b>	<b>DESCRIPTION</b>
31	0	RW	WMAA0E WAN MAC Additional Station Address 0 Enable When set, the additional WAN MAC address is enabled for received frames. When reset, the additional WAN MAC address is disabled.
30:16	0	RO	Reserved
15:0	--	RW	WMAAH0 WAN MAC Additional Station Address 0 High 2 bytes The most significant word of the additional WAN MAC 0 station address.

The following table shows the register map for all 16 additional WAN MAC address registers.

<b>REGISTER</b>	<b>IDENTIFIER</b>	<b>OFFSET</b>
ADD MAC Low 0	WMAAL0	0x6080
ADD MAC High 0	WMAAH0	0x6084
ADD MAC Low 1	WMAAL1	0x6088

ADD MAC High 1	WMAAH1	0x608C
ADD MAC Low 2	WMAAL2	0x6090
ADD MAC High 2	WMAAH2	0x6094
ADD MAC Low 3	WMAAL3	0x6098
ADD MAC High 3	WMAAH3	0x609C
ADD MAC Low 4	WMAAL4	0x60A0
ADD MAC High 4	WMAAH4	0x60A4
ADD MAC Low 5	WMAAL5	0x60A8
ADD MAC High 5	WMAAH5	0x60AC
ADD MAC Low 6	WMAAL6	0x60B0
ADD MAC High 6	WMAAH6	0x60B4
ADD MAC Low 7	WMAAL7	0x60B8
ADD MAC High 7	WMAAH7	0x60BC
ADD MAC Low 8	WMAAL8	0x60C0
ADD MAC High 8	WMAAH8	0x60C4
ADD MAC Low 9	WMAAL9	0x60C8
ADD MAC High 9	WMAAH9	0x60CC
ADD MAC Low 10	WMAAL10	0x60D0
ADD MAC High 10	WMAAH10	0x60D4
ADD MAC Low 11	WMAAL11	0x60D8
ADD MAC High 11	WMAAH11	0x60DC
ADD MAC Low 12	WMAAL12	0x60E0
ADD MAC High 12	WMAAH12	0x60E4
ADD MAC Low 13	WMAAL13	0x60E8
ADD MAC High 13	WMAAH13	0x60EC
ADD MAC Low 14	WMAAL14	0x60F0
ADD MAC High 14	WMAAH14	0x60F4
ADD MAC Low 15	WMAAL15	0x60F8
ADD MAC High 15	WMAAH15	0x60FC

### 3.4 LAN DMA Registers

#### 3.4.1 LAN MAC DMA Transmit Control Register (LMDTXC Offset 0x8000)

The LAN MAC DMA transmit control register establishes the transmit operating modes and commands for the LAN port. This register should be one of the last SCRs to be written as part of the transmit initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	WO	LMTRST LAN DMA Soft Reset When set, the LAN MAC DMA block is reset.



			All registers in the LAN MAC DMA block will be reset to the default values.
30		RO	Reserved
29:24	0	RW	LMTBS LAN DMA Transmit Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the LAN MAC DMA burst size is limited only by the amount of data stored in the transmit buffer before issuing a bus request. The LMTBS can be programmed with permissible values 0,1, 2, 4, 8, 16, or 32. After reset, the LMTBS default is 0, i.e. unlimited.
23:19	0	RO	Reserved
18	0	RW	LMTUCG LAN MAC Transmit UDP Checksum Generate When set, the KS8695X will generate correct UDP checksum for outgoing UDP/IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
17	0	RW	LMTTCG LAN MAC Transmit TCP Checksum Generate When set, the KS8695X will generate correct TCP checksum for outgoing TCP/IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
16	0	RW	LMTICG LAN MAC Transmit IP Checksum Generate When set, the KS8695X will generate correct IP checksum for outgoing IP frames at LAN port. When this bit is set, ADD CRC should also turn on.
15:10	0	RO	Reserved
9	0	RW	LMTFCE LAN MAC Transmit Flow Control Enable When this bit is set and the KS8695X is in Full Duplex mode, flow control is enabled and the KS8695X will transmit a PAUSE frame when the MAC DMA Receive Buffer capacity has reached a level that may cause the buffer to overflow. When this bit is set and the KS8695X is in Half Duplex mode, back-pressure flow control is enabled. When this bit is cleared, no transmit flow control is enabled.
8	0	RW	LMTLB LAN MAC DMA Loop Back Mode Select the KS8695X LAN port in loopback operation modes. When set, the packet to be sent will be returned at the MAC interface.
7:3	0	RO	Reserved
2	0	RW	LMTEP LAN MAC DMA Transmit Enable Padding When set, the KS8695X automatically adds a padding field to a packet shorter than 64 bytes. Note: Setting this bit automatically enables Add CRC feature.
1	0	RW	LMTAC LAN MAC DMA Transmit Add CRC When set, the KS8695X appends the CRC to the end of the transmission frame.
0	0	RW	LMTE LAN MAC DMA TX Enable When the bit is set, the DMA TX block is enabled and placed in a running state. When reset, the transmission process is placed in the stopped state after completing the transmission of the current frame. The stop transmission command is effective only when the transmission process is in the running state.

### 3.4.2 LAN MAC DMA Receive Control Register (LMDRXC Offset 0x8004)

The LAN MAC DMA receive control register establishes the receive operating modes and commands for the LAN port. This register should be one of the last SCRs to be written as part of the receive initialization.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:30	0	RO	Reserved
29:24	0	RW	LMRBS LAN DMA Receive Burst Size This field indicates the maximum number of words to be transferred in one DMA transaction. If reset, the LAN MAC DMA burst size is limited only by the amount of data stored in the receive buffer before issuing a bus request. The LMRBS can be programmed with permissible values 0,1, 2, 4, 8, 16, or 32. After reset, the LMRBS default is 0, i.e. unlimited.
23:19	0	RO	Reserved
18	0	RW	LMRUCC LAN MAC Receive UDP Checksum Check When set, the KS8695X will check for correct UDP checksum for incoming UDP/IP frames at LAN port. Packets received with incorrect UDP checksum will be discarded.
17	0	RW	LMRTCG LAN MAC Receive TCP Checksum Check When set, the KS8695X will check for correct TCP checksum for incoming TCP/IP frames at LAN port. Packets received with incorrect TCP checksum will be discarded.
16	0	RW	LMRICG LAN MAC Receive IP Checksum Check When set, the KS8695X will check for correct IP checksum for incoming IP frames at LAN port. Packets received with incorrect IP checksum will be discarded.
15:10	0	RO	Reserved
9	0	RW	LMRFCE LAN MAC Receive Flow Control Enable When this bit is set and the KS8695X is in Full Duplex mode, flow control is enabled and the KS8695X will acknowledge a PAUSE frame from the LAN port, i.e. the outgoing packets will be pending in the transmit buffer until the PAUSE control timer expires. This field has no meaning in half-duplex mode and should be programmed to 0. When this bit is cleared, no flow control is enabled.
8:7	0	RO	Reserved
6	0	RW	LMRB LAN MAC Receive Broadcast When set, the LAN MAC receive all broadcast frames.
5	0	RW	LMRM LAN MAC Receive Multicast When set, the LAN MAC receive all multicast frames (including broadcast).
4	0	RW	LMRU LAN MAC Receive Unicast When set, the LAN MAC receive unicast frames that match the 48-bit Station Address of the LAN MAC.
3	0	RW	LMRE LAN MAC DMA Receive Error Frame When set, the KS8695X will pass the errors frames received to the host. Error frames include runt frames, oversized frames, CRC errors.
2	0	RW	LMRA LAN MAC DMA Receive All When set, the KS8695X receives all incoming frames, regardless of its destination address.
1	0	RO	Reserved
0	0	RW	LMRE LAN MAC DMA RX Enable When the bit is set, the DMA RX block is enabled and placed in a running state. When reset, the receive process is placed in the stopped state after completing the reception of the current frame. The stop transmission command is effective only when the reception process is in the running state.

### 3.4.3 LAN MAC DMA Transmit Start Command Register (LMDTSC Offset 0x8008)

This register is written by the the CPU when packets in the LAN data buffer need to be transmitted.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0	WO	LTSC LAN Transmit Start Command When written with any value, the LAN Transmit DMA checks for frames to be transmitted. If no descriptor is available, the transmit process returns to suspended state. If descriptors are available, the transmit process starts or resumes. This bit is self-clearing.

### 3.4.4 LAN MAC DMA Receive Start Command Register (LMDRSC Offset 0x800C)

This register is written by the the CPU when there are frame data in receive buffer to be processed.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0	WO	LRSC LAN Receive Start Command When written with any value, the WLAN Receive DMA checks for descriptors to be acquired. If no descriptor is available, the receive process returns to suspended state and wait for the next receive restart command. If descriptors are available, the receive process resumes. This bit is self-clearing.

### 3.4.5 LAN Transmit Descriptor List Base Address Register (LTDLB Offset 0x8010)

This register is used for LAN Transmit descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695X behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0	RW	LSTL LAN Start of Transmit List Note: Write can only occur when the transmit process stopped.
1:0	0	RO	Reserved

### 3.4.6 LAN Receive Descriptor List Base Address Register (LRDLB Offset 0x8014)

This register is used for LAN Receive descriptor list base address register. The register is used to point to the start of the appropriate descriptor list. Writing to this register is permitted only when its respective process is in the stopped state. When stopped, the register must be written before the respective **START** command is given.

Note: The descriptor lists must be Word (32-bit) aligned. The KS8695X behavior is unpredictable when the lists are not word-aligned.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0	RW	LSRL LAN Start of Receive List Note: Write can only occur when the transmit process stopped.
1:0	0	RO	Reserved

### 3.4.7 LAN MAC Station Address Low Register (LMAL Offset 0x8018)

Station Address is used to define the individual destination address the KS8695X LAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0	RW	LMAL LAN MAC Station Address Low 4 bytes The least significant word of the LAN MAC station address.

### 3.4.8 LAN MAC Station Address High Register (LMAH Offset 0x801C)

Station Address is used to define the individual destination address the KS8695X LAN port will respond to when receiving frames. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0	RO	Reserved
15:0	0	RW	LMAL LAN MAC Station Address High 2 bytes The most significant word of the LAN MAC station address.

### 3.4.9 LAN MAC Additional Station Address Low Register (LMAAL0-15)

The KS8695X supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695X will respond to when receiving frames on the LAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	LMAAL0 LAN MAC Additional Station Address 0 Low 4 bytes The least significant word of the additional LAN MAC 0 station address.

### 3.4.10 LAN MAC Additional Station Address High Register (LMAAH0-15)

The KS8695X supports 16 additional MAC addresses for MAC address filtering. This MAC address is used to define one of the 16 destination addresses that the KS8695X will respond to when receiving frames on the LAN port. Network addresses are generally expressed in the form of 01:23:45:67:89:AB, where the bytes are received left to right, and the bits within each byte are received right to left (LSB to MSB). The actual transmitted and received bits are in the order of 10000000 11000100 10100010 11100110 10010001 11010101.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	LMAA0E LAN MAC Additional Station Address 0 Enable When set, the additional LAN MAC address is enabled for received frames. When reset, the additional LAN MAC address is disabled.
30:16	0	RO	Reserved
15:0	--	RW	LMAAH0 LAN MAC Additional Station Address 0 High 2 bytes The most significant word of the additional LAN MAC 0 station address.

The following table shows the register map for all 16 additional LAN MAC address registers.

REGISTER	IDENTIFIER	OFFSET
ADD MAC Low 0	LMAAL0	0x8080
ADD MAC High 0	LMAAH0	0x8084
ADD MAC Low 1	LMAAL1	0x8088
ADD MAC High 1	LMAAH1	0x808C
ADD MAC Low 2	LMAAL2	0x8090
ADD MAC High 2	LMAAH2	0x8094
ADD MAC Low 3	LMAAL3	0x8098
ADD MAC High 3	LMAAH3	0x809C
ADD MAC Low 4	LMAAL4	0x80A0
ADD MAC High 4	LMAAH4	0x80A4
ADD MAC Low 5	LMAAL5	0x80A8
ADD MAC High 5	LMAAH5	0x80AC
ADD MAC Low 6	LMAAL6	0x80B0
ADD MAC High 6	LMAAH6	0x80B4
ADD MAC Low 7	LMAAL7	0x80B8
ADD MAC High 7	LMAAH7	0x80BC
ADD MAC Low 8	LMAAL8	0x80C0

ADD MAC High 8	LMAAH8	0x80C4
ADD MAC Low 9	LMAAL9	0x80C8
ADD MAC High 9	LMAAH9	0x80CC
ADD MAC Low 10	LMAAL10	0x80D0
ADD MAC High 10	LMAAH10	0x80D4
ADD MAC Low 11	LMAAL11	0x80D8
ADD MAC High 11	LMAAH11	0x80DC
ADD MAC Low 12	LMAAL12	0x80E0
ADD MAC High 12	LMAAH12	0x80E4
ADD MAC Low 13	LMAAL13	0x80E8
ADD MAC High 13	LMAAH13	0x80EC
ADD MAC Low 14	LMAAL14	0x80F0
ADD MAC High 14	LMAAH14	0x80F4
ADD MAC Low 15	LMAAL15	0x80F8
ADD MAC High 15	LMAAH15	0x80FC

## 3.5 UART Registers

### 3.5.1 UART Receive Buffer Register (URRB Offset 0xE000)

The UART Receive Buffer register contains an 8-bit data value received over the UART channel.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:0	--	RO	URRBD UART Receive Buffer Data This field contains the data received over the single channel UART. When UART finishes receiving data frame, the Receive Data Ready bit in the Line Status Register will be set. Note: whenever the URRBD is read, the Receive Data Ready bit in the Line Status Register is automatically cleared.

### 3.5.2 UART Transmit Holding Register (URTH Offset 0xE004)

The UART Transmit Holding register contains an 8-bit data value to be transmitted over the UART channel.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:0	--	WO	URTHD UART Transmit Holding Data This field contains the data to be transmitted over the single channel UART. Whenever the URTHD is written, the Transmit Holding Register Empty bit in the Line Status Register is automatically cleared to '0' until the UART finishes transmitting the data.



			Note: software should ensure that the Transmit Holding Register Empty bit in the Line Status Register is '1' before writing to this register to prevent from over-writing the current transmit data.
--	--	--	--

### 3.5.3 UART FIFO Control Register (URFC Offset 0xE008)

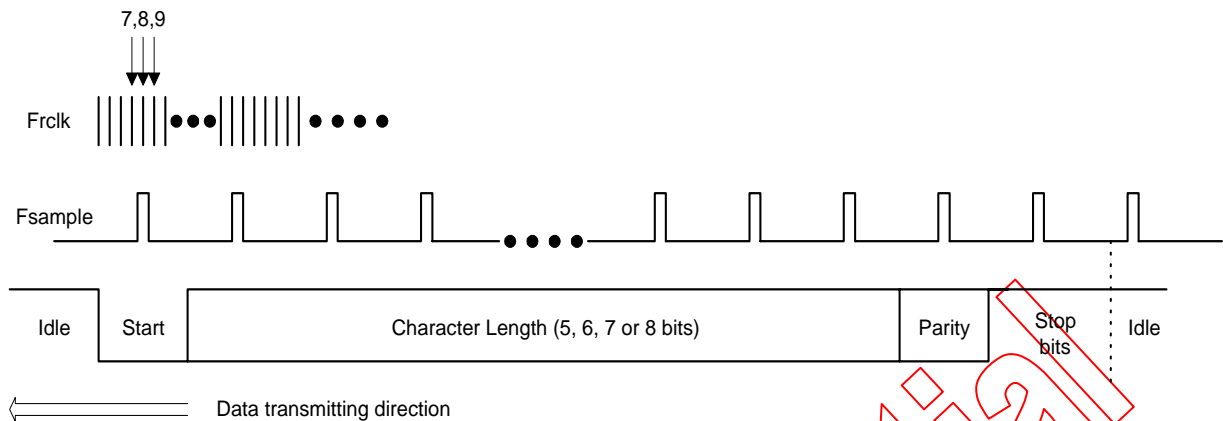
The UART FIFO Control register provides control over transmitter and receiver FIFOs.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:6	0	RW	URFRT UART Receive FIFO Trigger Level This field controls the trigger level for the receive FIFO. 00 = 1 Byte 01 = 4 Bytes 10 = 8 Bytes 11 = 14 Bytes
5:3	0	RO	Reserved
2	0	RW	URTFR UART Transmit FIFO Reset When set, the transmit state machine will be reset, and the transmit FIFO will be emptied. Writing '0' has no effect. Note: This bit will be self-cleared to 0 after 1 is written.
1	0	RW	URRFR UART Receive FIFO Reset When set, the receive FIFO state machine will be reset, and receive FIFO will be emptied. Writing '0' has no effect. Note: This bit will be self-cleared to 0 after 1 is written.
0	0	RW	URFE UART FIFO Enable When set, both the transmit and receive FIFOs are enabled. (UART is in 16550 mode) When reset, both the transmit and receive FIFOs are disabled. (UART is in 16450 mode) Note that when UART changes from FIFO to character mode or vice versa, data in the FIFOs are automatically cleared. This bit must be set when other control bits in this register are written to or they will not be programmed.

### 3.5.4 UART Line Control Register (URLC Offset 0xE00C)

The UART Line Control register basically specifies the asynchronous data frame for transmitting and receiving as seen below.



When the bus(one bit serial bus) is idle, it stays at high. The first high-to-low transition is detected as the Start bit. Start bit is Low and Stop bit is High. Due to the noise, a short glitch might happen on the bus. To avoid detecting the wrong Start bit, three samples at clock (Frclk) 7, 8, and 9 after high-to-low transition is taken on the bus. If at least two out of three samples are Low, then Start bit is detected; otherwise, the high-to-low transition is treated as a glitch. Frclk and Fsample will be defined at Baud Rate Divisor Register section.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:7	0	RO	Reserved
6	0	RW	URSBC UART Set Break Condition on UTXD When set, a break condition will be asserted on the UTXD pin. A break condition is when the UTXD is driven low for more than one frame time ( including Start, Parity, and Stop bits) measured at a give baud rate.
5	0	RW	URSPB UART Stick Parity Bit When set, the stick parity is enabled, ( stick parity has precedence over even/odd parity), i.e. if bit URPE, UREPb, and URSPB are all 1's, parity is always 0. If bits URPE, and URSPB are 1's, and bit UREPb is 0, parity is always 1. When reset, stick parity is disabled.
4	0	RW	UREPB UART Even Parity Bit 1 = even parity. 0 = odd parity.
3	0	RW	URPE UART Parity Enable (Even/Odd/Stick) When set, parity is enabled. When reset, parity is disabled.
2	0	RW	URSB UART Stop Bits 0 = 1 Stop bit per data frame. 1 = 2 Stop bit per data frame.
1:0	0	RW	URCL UART Character Length 00 = 5 data bits per frame. 01 = 6 data bits per frame. 10 = 7 data bits per frame. 11 = 8 data bits per frame.



### 3.5.5 UART Modem Control Register (URMC Offset 0xE010)

The UART Modem Control register provides interface with the MODEM. All the UART and Modem communication uses software handshaking.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:5	0	RO	Reserved
4	0	RW	URLB UART Loop Back Mode When set, the UART is in the local loopback mode. This feature is for software diagnostics/testing. When reset, the UART is in normal functional mode. Note: In the UART loopback mode, the interrupt mechanism is fully operational. The operation of the Modem in the loopback mode is similar to external Modem loopback with Null modem cable.
3	0	RW	UROUT2 UART OUT2 When set, the internal UART OUT2 signal is asserted to 0. When reset, the internal UART OUT2 signal is deasserted.
2	0	RW	UROUT1 UART OUT1 When set, the internal UART OUT1 signal is asserted to 0. When reset, the internal UART OUT1 signal is deasserted.
1	0	RW	URRTS UART Request To Send When set, the UART RTS pin is asserted to 0. When reset, the UART RTS pin is deasserted.
0	0	RW	URDTR UART Data Terminal Ready When set, the UART DTR pin is asserted to 0. When reset, the UART DTR pin is deasserted.

### 3.5.6 UART Line Status Register (URLS Offset 0xE014)

The UART Line Status register provides status information to the CPU regarding the received data. The receive FIFO has 16 entries, each of which includes one byte of data and three error bits (parity error, framing error, and break interrupt) associated to the data. The Line status register is read only; writing to this register has no effect.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7	0	RO	URRFE UART Receive FIFO Error This bit is meaningful only in FIFO mode to indicate that the UART receive FIFO contains error(s). Reading of '1' indicates there is at least one of the following errors: parity error, framing error, or break interrupt. This bit is cleared only when it is read by CPU and no subsequent errors in the FIFO.
6	1	RO	URTE UART Transmit Empty This bit indicates that the UART Transmit buffer is ready to accept new data for transmit. In character mode (16450): When set to '1', it indicates that the Transmit Holding Register and Transmitter Shift

			<p>Register are both empty.</p> <p>In FIFO mode (16550):</p> <p>When set to '1', it indicates that both the Transmit FIFO and Transmit Shift Register are empty</p>
5	1	RO	<p>URTHRE UART Transmit Holding Register Empty</p> <p>This bit indicates that the UART Transmit Holding Register (THR) is empty.</p> <p>In character mode (16450):</p> <p>When set to '1', it indicates the THR is empty.</p> <p>In FIFO mode (16550):</p> <p>When set to '1', it indicates that the Transmit FIFO is empty.</p>
4	0	RO	<p>URBI UART Break Interrupt Indicator</p> <p>In character mode (16450):</p> <p>When set, it indicates a "break" condition occurs on the URXD pin. A break condition is when the serial data is driven low for more than one frame time (including Start, Parity, and Stop bits) measured at a give baud rate.</p> <p>In FIFO mode (16550):</p> <p>The break interrupt bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit is reset to '0' when read.</p>
3	0	RO	<p>URFE UART Framing Error</p> <p>In character mode (16450):</p> <p>When set, the received character does not have the correct stop bit.( '0' is sampled)</p> <p>In FIFO mode (16550):</p> <p>The framing error bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit reset to '0' when read.</p>
2	0	RO	<p>URPE UART Parity Error</p> <p>In character mode (16450):</p> <p>When set, the received character does not have the correct even or odd parity (excluding stick parity), as selected by the parity select bit.</p> <p>In FIFO mode (16550):</p> <p>The parity error bit in the Receiver FIFO will be copied to this register bit when its associated character is at the top of the Receiver FIFO.</p> <p>This bit reset to '0' when read.</p>
1	0	RO	<p>URROE UART Receive Overrun Error</p> <p>In character mode (16450):</p> <p>When set, the Receive Buffer Register (RBR) has not been read by the CPU before the next character is ready to be transferred into RBR from the Receive Shift Register.</p> <p>In FIFO mode (16550):</p> <p>The Receiver FIFO is full and the next character is ready to be transferred into FIFO from the Receive Shift Register.</p> <p>This bit reset to '0' when read.</p>
0	0	RO	<p>URDR UART Receive Data Ready</p> <p>In character mode (16450):</p> <p>When set, data is valid in the Receive Buffer Register.</p> <p>In FIFO mode (16550):</p> <p>There is at least one character data ready in the Receive FIFO (not empty.)</p> <p>This bit will be cleared when no data in Receive Buffer Register or FIFO.</p>

### 3.5.7 UART Modem Status Register (URMS Offset 0xE018)

This register provides the current state of the Modem input control lines to the CPU. In addition to the current-state information, four bits of the Modem status register provide state-changing information. These bits are set to logic '1' whenever a control input from the remote Modem changes state. They are reset to '0' whenever the CPU reads the register. When either one of the four bits URLS[3:0] is set to '1', a Modem status interrupt is generated.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7	--	RO	URDCD UART Data Carrier Detect This bit indicates the logical (inverted) value of the UDCDN input.
6	--	RO	URRI UART Ring Indicator This bit indicates the logical (inverted) value of the URIN input pin.
5	--	RO	URDSR UART Data Set Ready This bit indicates the logical (inverted) value of the UDSRN input pin.
4	--	RO	URCTS UART Clear To Send This bit indicates the logical (inverted) value of the UCTSN input pin.
3	0	RO	URDDCD UART Delta Data Carrier Detect This bit is set when the UDCDN input pin has changed state. Cleared when read.
2	0	RO	URTERI UART Trailing Edge Ring Indicator This bit is set when the URIN input pin has changed from Low to High. Cleared when read.
1	0	RO	URDDST UART Delta Data Set Ready This bit is set when the UDSRN input pin has changed state. Cleared when read.
0	0	RO	URDCTS UART Delta Clear To Send This bit is set when the UCTSN input pin has changed state. Cleared when read.

### 3.5.8 UART Baud Rate Divisor Register (URBD Offset 0xE01C)

The input clock to the baud rate generator is fixed at 25MHz. This clock is divided by the value in the URBD register to generate the sample clock (Fsample), which is used to sample the incoming data or to drive the outgoing data. The frequency of Fclk is 16 times of Fsample.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0	RO	Reserved
23:0	1BE	RW	URBDC UART Baud Rate Divisor Count

### 3.5.9 UART Status Register (USR Offset 0xE020)

This register currently holds the Timeout Indication bit. The Timeout and Receive Triggered-level Reach shares the same interrupt Status(INTST[9]) bit. To further distinguish these two interrupt sources, a Timeout Indication bit is introduced.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:1	0	RO	Reserved
0	0	RO	UTI UART Timeout Indication bit If INTST[9] = 1 and USR[0] = 1, the interrupt source is from timeout. If INTST[9] = 1 and USR[0] = 0, the interrupt source is because the Receive FIFO has reached the trigger-level. Note that this bit will be automatically cleared when either a new coming frame has received or CPU reads Receive FIFO.

## 3.6 Interrupt Controller Registers

The KS8695X supports multiple interrupt sources with reconfigurable priority. Interrupt requests can be generated by internal functional blocks as well as external pins. The ARM core recognizes two kinds of interrupts: a normal interrupt request (IRQ), and a fast interrupt request (FIQ). All interrupts can be categorized as either IRQ or FIQ. The KS8695X interrupt controller has an interrupt status bit for each interrupt source. This register defines the interrupt source for each device interrupt.

In general, four special registers are used to control interrupt generation and handling:

- Interrupt Mode Control Register: defines the interrupt source to the ARM core to be IRQ or FIQ.
- Interrupt Priority Register: the index number of each interrupt source is written to the pre-defined interrupt priority register field to obtain the priority. The interrupt priorities are predefined from 0 to 15.
- Interrupt Status Register: indicates the interrupt status.
- Interrupt Enable Register: enables the interrupts.

### 3.6.1 Interrupt Mode Control Register (INTMC Offset 0xE200)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCIM WAN MAC Link Changed Interrupt Mode When set, the WAN MAC Link Change Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Link Change Interrupt corresponds to the IRQ (normal interrupt).
30	0	RW	WMTIM WAN MAC Transmit Interrupt Mode When set, the WAN MAC Transmit Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Transmit Interrupt corresponds to the IRQ (normal interrupt).
29	0	RW	WMRIM WAN MAC Receive Interrupt Mode When set, the WAN MAC Receive Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Receive Interrupt corresponds to the IRQ (normal interrupt).
28	0	RW	WMTBUIM WAN MAC Transmit Buffer Unavailable Interrupt Mode When set, the WAN MAC Transmit Buffer Unavailable Interrupt corresponds to the FIQ

			(fast Interrupt). When reset, the WAN MAC Transmit Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
27	0	RW	WMRBUIM WAN MAC Receive Buffer Unavailable Interrupt Mode When set, the WAN MAC Receive Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt). When reset, the WAN MAC Receive Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
26	0	RW	WMTPSIM WAN MAC Transmit Process Stopped Interrupt Mode When set, the WAN MAC Transmit Process Stopped Interrupt corresponds to the FIQ (fast interrupt). When reset, the WAN MAC Transmit Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
25	0	RW	WMRPSIM WAN MAC Receive Process Stopped Interrupt Mode When set, the WAN MAC Receive Process Stopped Interrupt corresponds to the FIQ (fast interrupt). When reset, the WAN MAC Receive Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
24	0	RW	ABERIM AMBA Bus Error Response Interrupt Mode When set, the AMBA Bus Error Response Interrupt corresponds to the FIQ (fast interrupt). When reset, the AMBA Bus Error Response Interrupt corresponds to the IRQ (normal interrupt).
23	0	RW	Reserved. For factory test purpose only.
22	0	RW	Reserved. For factory test purpose only.
21	0	RW	Reserved. For factory test purpose only.
20	0	RW	Reserved. For factory test purpose only.
19	0	RW	Reserved. For factory test purpose only.
18	0	RW	Reserved. For factory test purpose only.
17	0	RW	LMTIM LAN MAC Transmit Interrupt Mode When set, the LAN MAC Transmit Interrupt corresponds to the FIQ (fast Interrupt). When reset, the LAN MAC Transmit Interrupt corresponds to the IRQ (normal interrupt).
16	0	RW	LMRIM LAN MAC Receive Interrupt Mode When set, the LAN MAC Receive Interrupt corresponds to the FIQ (fast Interrupt). When reset, the LAN MAC Receive Interrupt corresponds to the IRQ (normal interrupt).
15	0	RW	LMTBUIM LAN MAC Transmit Buffer Unavailable Interrupt Mode When set, the LAN MAC Transmit Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt). When reset, the LAN MAC Transmit Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
14	0	RW	LMRBUIM LAN MAC Receive Buffer Unavailable Interrupt Mode When set, the LAN MAC Receive Buffer Unavailable Interrupt corresponds to the FIQ (fast Interrupt). When reset, the LAN MAC Receive Buffer Unavailable Interrupt corresponds to the IRQ (normal interrupt).
13	0	RW	LMTPSIM LAN MAC Transmit Process Stopped Interrupt Mode When set, the LAN MAC Transmit Process Stopped Interrupt corresponds to the FIQ (fast interrupt). When reset, the LAN MAC Transmit Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
12	0	RW	LMRPSIM LAN MAC Receive Process Stopped Interrupt Mode When set, the LAN MAC Receive Process Stopped Interrupt corresponds to the FIQ (fast

			interrupt). When reset, the LAN MAC Receive Process Stopped Interrupt corresponds to the IRQ (normal interrupt).
11	0	RW	MSIM Modem Status Interrupt Mode When set, the Modem status Interrupt corresponds to the FIQ (fast interrupt). When reset, the Modem status Interrupt corresponds to the IRQ (normal interrupt). Modem status is defined as logic OR of the following Modem conditions: Clear to Send, Data Set Ready, Ring Indicator, Data Carrier Detect.
10	0	RW	ULESM UART Line Error Status Mode When set, the UART Line Error Status Interrupt corresponds to the FIQ (fast interrupt). When reset, the UART Line Error Status Interrupt corresponds to the IRQ (normal interrupt). UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.
9	0	RW	URIM UART Receive Interrupt Mode When set, the UART receive interrupt corresponds to the FIQ (fast interrupt). When reset, the UART receive interrupt corresponds to the IRQ (normal interrupt).
8	0	RW	UTIM UART Transmit Interrupt Mode When set, the UART transmit interrupt corresponds to the FIQ (fast interrupt). When reset, the UART transmit interrupt corresponds to the IRQ (normal interrupt).
7	0	RW	TI1M Timer 1 Interrupt Mode When set, the Timer 1 Interrupt corresponds to the FIQ (fast interrupt). When reset, the Timer 1 Interrupt corresponds to the IRQ (normal interrupt).
6	0	RW	TOIM Timer 0 Interrupt Mode When set, the Timer 0 Interrupt corresponds to the FIQ (fast interrupt). When reset, the Timer 0 Interrupt corresponds to the IRQ (normal interrupt).
5	0	RW	EXTI3M External Interrupt 3 Mode When set, the external interrupt 3 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 3 corresponds to the IRQ (normal interrupt).
4	0	RW	EXTI2M External Interrupt 2 Mode When set, the external interrupt 2 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 2 corresponds to the IRQ (normal interrupt).
3	0	RW	EXTI1M External Interrupt 1 Mode When set, the external interrupt 1 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 1 corresponds to the IRQ (normal interrupt).
2	0	RW	EXTI0M External Interrupt 0 Mode When set, the external interrupt 0 corresponds to the FIQ (fast interrupt). When reset, the external interrupt 0 corresponds to the IRQ (normal interrupt).
1	0	RW	CCTM Communications Channel Transmit Mode When set, the communications channel transmit corresponds to the FIQ (fast interrupt). When reset, the communications channel transmit corresponds to the IRQ (normal interrupt).
0	0	RW	CCRM Communications Channel Receive Mode When set, the communications channel receive corresponds to the FIQ (fast interrupt). When reset, the communications channel receive corresponds to the IRQ (normal interrupt).



### 3.6.2 Interrupt Enable Register (INTEN Offset 0xE204)

This register enables the interrupts from the internal or external sources.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCIE WAN MAC Link Changed Interrupt Enable When this bit is set, the WAN MAC Link Changed Interrupt is enabled. When this bit is reset, the WAN MAC Link Changed Interrupt is disabled.
30	0	RW	WMTIE WAN MAC Transmit Interrupt Enable When this bit is set, the WAN MAC Transmit Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Interrupt is disabled.
29	0	RW	WMRIE WAN MAC Receive Interrupt Enable When this bit is set, the WAN MAC Receive Interrupt is enabled. When this bit is reset, the WAN MAC Receive Interrupt is disabled.
28	0	RW	WMTBUIE WAN MAC Transmit Buffer Unavailable Interrupt Enable When this bit is set, the WAN MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Buffer Unavailable Interrupt is disabled.
27	0	RW	WMRBUIE WAN MAC Receive Buffer Unavailable Interrupt Enable When this bit is set, the WAN MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the WAN MAC Receive Buffer Unavailable Interrupt is disabled.
26	0	RW	WMTPSIE WAN MAC Transmit Process Stopped Interrupt Enable When this bit is set, the WAN MAC Transmit Process Stopped Interrupt is enabled. When this bit is reset, the WAN MAC Transmit Process Stopped Interrupt is disabled.
25	0	RW	WMRPSIE WAN MAC Receive Process Stopped Interrupt Enable When this bit is set, the WAN MAC Receive Process Stopped Interrupt is enabled. When this bit is reset, the WAN MAC Receive Process Stopped Interrupt is disabled.
24	0	RW	ABERIE AMBA Bus Error Response Interrupt Enable When this bit is set, the AMBA Bus Error Response Interrupt is enabled. When this bit is reset, the AMBA Bus Error Response Interrupt is disabled.
23	0	RW	Reserved. For factory test purpose only.
22	0	RW	Reserved. For factory test purpose only.
21	0	RW	Reserved. For factory test purpose only.
20	0	RW	Reserved. For factory test purpose only.
19	0	RW	Reserved. For factory test purpose only.
18	0	RW	Reserved. For factory test purpose only.
17	0	RW	LMTIE LAN MAC Transmit Interrupt Enable When this bit is set, the LAN MAC Transmit Interrupt is enabled. When this bit is reset, the LAN MAC Transmit Interrupt is disabled.
16	0	RW	LMRIE LAN MAC Receive Interrupt Enable When this bit is set, the LAN MAC Receive Interrupt is enabled. When this bit is reset, the LAN MAC Receive Interrupt is disabled.
15	0	RW	LMTBUIE LAN MAC Transmit Buffer Unavailable Interrupt Enable When this bit is set, the LAN MAC Transmit Buffer Unavailable Interrupt is enabled. When this bit is reset, the LAN MAC Transmit Buffer Unavailable Interrupt is disabled.
14	0	RW	LMRBUIE LAN MAC Receive Buffer Unavailable Interrupt Enable When this bit is set, the LAN MAC Receive Buffer Unavailable Interrupt is enabled. When this bit is reset, the LAN MAC Receive Buffer Unavailable Interrupt is disabled.

13	0	RW	<p>LMTPSIE LAN MAC Transmit Process Stopped Interrupt Enable</p> <p>When this bit is set, the LAN MAC Transmit Process Stopped Interrupt is enabled.</p> <p>When this bit is reset, the LAN MAC Transmit Process Stopped Interrupt is disabled.</p>
12	0	RW	<p>LMRPSIE LAN MAC Receive Process Stopped Interrupt Enable</p> <p>When this bit is set, the LAN MAC Receive Process Stopped Interrupt is enabled.</p> <p>When this bit is reset, the LAN MAC Receive Process Stopped Interrupt is disabled.</p>
11	0	RW	<p>MSIE Modem Status Interrupt Enable</p> <p>When this bit is set, the Modem status Interrupt is enabled.</p> <p>When this bit is reset, the Modem status Interrupt is disabled.</p> <p>Modem status is defined as logic OR of the following Modem conditions: Clear to Send, Data Set Ready, Ring Indicator, Data Carrier Detect.</p>
10	0	RW	<p>ULESE UART Line Error Status Enable</p> <p>When this bit is set, the UART Line Error Status Interrupt is enabled.</p> <p>When this bit is reset, the UART Line Error Status Interrupt is disabled.</p> <p>UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.</p>
9	0	RW	<p>URIE UART Receive Interrupt Enable</p> <p>When this bit is set, the UART receive interrupt is enabled.</p> <p>When this bit is reset, the UART receive interrupt is disabled.</p>
8	0	RW	<p>UTIE UART Transmit Interrupt Enable</p> <p>When this bit is set, the UART transmit interrupt is enabled.</p> <p>When this bit is reset, the UART transmit interrupt is disabled.</p>
7	0	RW	<p>TIIM Timer 1 Interrupt Enable</p> <p>When this bit is set, the Timer 1 Interrupt is enabled.</p> <p>When this bit is reset, the Timer 1 Interrupt is disabled.</p>
6	0	RW	<p>TOIM Timer 0 Interrupt Enable</p> <p>When this bit is set, the Timer 0 Interrupt is enabled.</p> <p>When this bit is reset, the Timer 0 Interrupt is disabled.</p>
5	0	RW	<p>EXTI3 External Interrupt 3 Enable</p> <p>When this bit is set, the external interrupt 3 is enabled.</p> <p>When this bit is reset, the external interrupt 3 is disabled.</p>
4	0	RW	<p>EXTI2 External Interrupt 2 Enable</p> <p>When this bit is set, the external interrupt 2 is enabled.</p> <p>When this bit is reset, the external interrupt 2 is disabled.</p>
3	0	RW	<p>EXTI1 External Interrupt 1 Enable</p> <p>When this bit is set, the external interrupt 1 is enabled.</p> <p>When this bit is reset, the external interrupt 1 is disabled.</p>
2	0	RW	<p>EXTI0 External Interrupt 0 Enable</p> <p>When this bit is set, the external interrupt 0 is enabled.</p> <p>When this is reset, the external interrupt 0 is disabled.</p>
1	0	RW	<p>CCTE Communications Channel Transmit Enable</p> <p>When this bit is set, the Communications Channel Transmit is enabled.</p> <p>When this is reset, the Communications Channel Transmit is disabled.</p>
0	0	RW	<p>CCRE Communications Channel Receive Enable</p> <p>When this bit is set, the Communications Channel Receive is enabled.</p> <p>When this is reset, the Communications Channel Receive is disabled.</p>



### 3.6.3 Interrupt Status Register (INTST Offset 0xE208)

This register contains all the status bits for the ARM CPU. When corresponding enable bit is set, it cause the CPU to be interrupted. This register is usually read by the driver during interrupt service routine or polling. The register bits are not cleared when read. Each field can be masked.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WMLCS WAN MAC Link Changed Status When this bit is set, it indicates that the WAN MAC link status has changed from link up to link down or from link down to link up. This edge-triggered interrupt status is cleared by writing 1 to this bit.
30	0	RW	WMTS WAN MAC Transmit Status When this bit is set, it indicates that the WAN MAC has transmitted at least a frame on the WAN port and the MAC is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
29	0	RW	WMRS WAN MAC Receive Status When this bit is set, it indicates that the WAN MAC has received a frame from the WAN port and it is ready for the host to process. This edge-triggered interrupt status is cleared by writing 1 to this bit.
28	0	RW	WMTBUS WAN MAC Transmit Buffer Unavailable Status When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KS8695. The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command. This edge-triggered interrupt status is cleared by writing 1 to this bit.
27	0	RW	WMRBUS WAN MAC Receive Buffer Unavailable Status When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KS8695. The receiving process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KS8695. This edge-triggered interrupt status is cleared by writing 1 to this bit.
26	0	RW	WMPSS WAN MAC Transmit Process Stopped Status Asserted when the WAN MAC transmit process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
25	0	RW	WMPSS WAN MAC Receive Process Stopped Status Asserted when the WAN MAC receive process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
24	0	RO	ABERS AMBA Bus Error Response Status When this bit is set, it indicates that either WAN or LAN AMBA master has received a bus error response from slave(memory controller). This level-triggered interrupt status is automatically cleared when interrupt source is cleared.
23	0	RW	Reserved. For factory test purpose only.
22	0	RW	Reserved. For factory test purpose only.
21	0	RW	Reserved. For factory test purpose only.
20	0	RW	Reserved. For factory test purpose only.
19	0	RW	Reserved. For factory test purpose only.

18	0	RW	Reserved. For factory test purpose only.
17	0	RW	<b>LMTS LAN MAC Transmit Status</b> When this bit is set, it indicates that the LAN MAC has transmitted at least a frame on the LAN port and the MAC is ready for new frames from the host. This edge-triggered interrupt status is cleared by writing 1 to this bit.
16	0	RW	<b>LMRS LAN MAC Receive Status</b> When this bit is set, it indicates that the LAN MAC has received a frame from the LAN port and it is ready for the host to process This edge-triggered interrupt status is cleared by writing 1 to this bit.
15	0	RW	<b>LMTBUS LAN MAC Transmit Buffer Unavailable Status</b> When this bit is set, it indicates that the next descriptor on the transmit list is owned by the host and cannot be acquired by the KS8695. The transmission process is suspended. To resume processing transmit descriptors, the host should change the ownership bit of the descriptor and then issue a transmit start command. This edge-triggered interrupt status is cleared by writing 1 to this bit.
14	0	RW	<b>LMRBUS LAN MAC Receive Buffer Unavailable Status</b> When this bit is set, it indicates that the descriptor list is owned by the host and cannot be acquired by the KS8695. The receiving process is suspended. To resume processing receive descriptors, the host should change the ownership of the descriptor and may issue a receive start command. If no receive start command is issued, the receiving process resumes when the next recognized incoming frame is received. After the first assertion, this bit is not asserted for any subsequent not owned receive descriptors fetches. This bit is asserted only when the previous receive descriptor was owned by the KS8695. This edge-triggered interrupt status is cleared by writing 1 to this bit.
13	0	RW	<b>LMT PSS LAN MAC Transmit Process Stopped Status</b> Asserted when the LAN MAC transmit process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
12	0	RW	<b>LMR PSS LAN MAC Receive Process Stopped Status</b> Asserted when the LAN MAC receive process enters the stopped state. This edge-triggered interrupt status is cleared by writing 1 to this bit.
11	0	RO	<b>UMS UART Modem Status</b> When this bit is set, it indicates that the UART modem status is set. UART modem status is defined as logic OR of Delta Data Carrier Detect, Trailing Edge Ring Indicator, Delta Data Set Ready and Delta Clear To Send. This level-triggered interrupt status is automatically cleared when UART Modem Status Register is read.
10	0	RO	<b>ULES UART Line Error Status</b> When this bit is set, it indicates that the UART line error status is set. UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt. This level-triggered interrupt status is automatically cleared when UART Line Status Register is read.
9	0	RO	<b>URS UART Receive Status</b> When this bit is set, it indicates that the UART receive status is set. UART receive status is defined as logic OR of received data available or character timeout indication. For received data available, it indicates Receive Buffer Register is full(character mode) or trigger-level reached(FIFO mode). This level-triggered interrupt status is automatically cleared when UART Receive Buffer Register is read or FIFO drops below trigger-level. For character timeout indication, it indicates timeout has occurred in FIFO mode. This level-triggered interrupt status is automatically cleared when CPU reads a datum back. Note that UART Status Register can provide further information if this interrupt status is for received data available or timeout.

8	1	RW	UTS UART Transmit Status When this bit is set, it indicates that the UART transmit status is set. UART transmit status is defined as the emptiness of Transmit Holding Register. This edge-triggered interrupt status is cleared by writing 1 to this bit.
7	0	RW	T1MS Timer 1 Status When this bit is set, it indicates that the Timer 1 status is set as specified in the Timer 1 registers. This edge-triggered interrupt status is cleared by writing 1 to this bit.
6	0	RW	T0MS Timer 0 Status When this bit is set, it indicates that the Timer 0 status is set as specified in the Timer 0 registers. This edge-triggered interrupt status is cleared by writing 1 to this bit.
5	0	RW	EXTI3S External Interrupt 3 Status When this bit is set, it indicates that the external interrupt 3 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
4	0	RW	EXTI2S External Interrupt 2 Status When this bit is set, it indicates that the external interrupt 2 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
3	0	RW	EXTI1S External Interrupt 1 Status When this bit is set, it indicates that the external interrupt 1 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
2	0	RW	EXTI0S External Interrupt 0 Status When this bit is set, it indicates that the external interrupt 0 pin is set. This interrupt status is cleared by writing 1 to this bit if edge-trigger is selected.
1	0	RO	CCTS Communications Channel Transmit Status. When this bit is set, it indicates that the Communications Channel Transmit pin is set. When High, this signal denotes that the comms channel transmit buffer is empty. This level-triggered interrupt status is automatically cleared when interrupt source is cleared.
0	0	RO	CCRS Communications Channel Receive Status. When this bit is set, it indicates that the Communications Channel Receive pin is set. When High, this signal denotes that the comms channel receive buffer contains data waiting to be read by the processor core. This level-triggered interrupt status is automatically cleared when interrupt source is cleared.

### 3.6.4 Interrupt Priority Register for WAN MAC (INTPW Offset 0xE20C)

This register configures the priority of the WAN DMA Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:28	0	RW	WMRIP WAN MAC Link Changed Interrupt Priority Level This field defines the priority level of the WAN MAC Link Changed Interrupt if enabled.
27:24	0	RW	WMTIP WAN MAC Transmit Interrupt Priority Level This field defines the priority level of the WAN MAC Transmit Interrupt if enabled.
23:20	0	RW	WMRIP WAN MAC Receive Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Interrupt if enabled.
19:16	0	RW	WMTBUIP WAN MAC Transmit Buffer Unavailable Interrupt Priority Level

			This field defines the priority level of the WAN MAC Transmit Buffer Unavailable Interrupt if enabled.
15:12	0	RW	WMTBUIP WAN MAC Receive Buffer Unavailable Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Buffer Unavailable Interrupt if enabled.
11:8	0	RW	WMTPSIP WAN MAC Transmit Process Stopped Interrupt Priority Level This field defines the priority level of the WAN MAC Transmit Process Stopped Interrupt if enabled.
7:4	0	RW	WMRPSIP WAN MAC Receive Process Stopped Interrupt Priority Level This field defines the priority level of the WAN MAC Receive Process Stopped Interrupt if enabled.
3:0	0	RO	Reserved

### 3.6.5 Interrupt Priority Register for LAN MAC (INTPL Offset 0xE214)

This register configures the priority of the LAN DMA Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:28	0	RW	Reserved.
27:24	0	RW	LMTIP LAN MAC Transmit Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Interrupt if enabled.
23:20	0	RW	LMRIP LAN MAC Receive Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Interrupt if enabled.
19:16	0	RW	LMTBUIP LAN MAC Transmit Buffer Unavailable Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Buffer Unavailable Interrupt if enabled.
15:12	0	RW	LMTBUIP LAN MAC Receive Buffer Unavailable Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Buffer Unavailable Interrupt if enabled.
11:8	0	RW	LMTPSIP LAN MAC Transmit Process Stopped Interrupt Priority Level This field defines the priority level of the LAN MAC Transmit Process Stopped Interrupt if enabled.
7:4	0	RW	LMRPSIP LAN MAC Receive Process Stopped Interrupt Priority Level This field defines the priority level of the LAN MAC Receive Process Stopped Interrupt if enabled.
3:0	0	RO	Reserved

### 3.6.6 Interrupt Priority Register for Timer (INTPT Offset 0xE218)

This register configures the priority of the Timer Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved

7:4	0	RW	T1IP Timer 1 Interrupt Priority Level This field defines the priority level of the Timer 1 Interrupt if enabled.
3:0	0	RW	T0IP Timer 0 Interrupt Priority Level This field defines the priority level of the Timer 0 Interrupt in enabled.

### 3.6.7 Interrupt Priority Register for UART (INTPU Offset 0xE21C)

This register configures the priority of the UART Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0	RO	Reserved
15:12	0	RW	MSIP Modem Status Interrupt Priority Level This field defines the priority level of the Modem Status Interrupt if enabled.
11:8	0	RW	ULESIP UART Line Error Status Interrupt Priority Level This field defines the priority level of the Line Error Status Interrupt if enabled.
7:4	0	RW	URIP UART Receive Interrupt Priority Level This field defines the priority level of the UART Receive Interrupt if enabled.
3:0	0	RW	UTIP UART Transmit Interrupt Priority Level This field defines the priority level of the UART Transmit Interrupt if enabled.

### 3.6.8 Interrupt Priority Register for External Interrupt (INTPE Offset 0xE220)

This register configures the priority of the External Interrupt sources. There are a total of 16 priority levels, 0xF has the highest priority; 0x0 has the lowest priority. Note that FIQ still has higher precedence over IRQ.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0	RO	Reserved
15:12	0	RW	EXTI3P External Interrupt 3 Priority Level This field defines the priority level of the External Interrupt 3 if enabled.
11:8	0	RW	EXTI2P External Interrupt 2 Priority Level This field defines the priority level of the External Interrupt 2 if enabled.
7:4	0	RW	EXTI1P External Interrupt 1 Priority Level This field defines the priority level of the External Interrupt 1 if enabled.
3:0	0	RW	EXTI0P External Interrupt 0 Priority Level This field defines the priority level of the External Interrupt 0 if enabled.

### 3.6.9 Interrupt Priority Register for Communications Channel (INTPC Offset 0xE224)

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:4	0	RW	CCTP Communications Channel Transmit Priority Level This field defines the priority level of the Communications Channel Transmit if enabled.
3:0	0	RW	CCRP Communications Channel Receive Priority Level This field defines the priority level of the Communications Channel Receive if enabled.

### 3.6.10 Interrupt Priority Register for Bus Error Response (INTPBE Offset 0xE228)

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:4	0	RO	Reserved
3:0	0	RW	ABERP AMBA Bus Error Response Priority Level This field defines the priority level of the Bus Error Response if enabled.

### 3.6.11 Interrupt Mask Status Register (INTMS Offset 0xE22C)

This register is the logical AND of the Interrupt Enable Register and the Interrupt Status Register. This register is read only.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIMS WAN MAC Link Change Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Link Change Interrupt is enabled and its corresponding status bit is set.
30	0	RO	WMTIMS WAN MAC Transmit Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Interrupt is enabled and its corresponding status bit is set.
29	0	RO	WMRIMS WAN MAC Receive Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Interrupt is enabled and its corresponding status bit is set.
28	0	RO	WMTBUMS WAN MAC Transmit Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
27	0	RO	WMRBUMS WAN MAC Receive Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
26	0	RO	WMTPSMS WAN MAC Transmit Process Stopped Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt is enabled and its corresponding status bit is set.



25	0	RO	WMRPSMS WAN MAC Receive Process Stopped Interrupt Mask Status When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt is enabled and its corresponding status bit is set.
24	0	RO	ABERMS AMBA Bus Error Response Interrupt Mask Status When this bit is set, it indicates that the AMBA Bus Error Response Interrupt is enabled and its corresponding status bit is set.
23	0	RO	Reserved. For factory test purpose only.
22	0	RO	Reserved. For factory test purpose only.
21	0	RO	Reserved. For factory test purpose only.
20	0	RO	Reserved. For factory test purpose only.
19	0	RO	Reserved. For factory test purpose only.
18	0	RO	Reserved. For factory test purpose only.
17	0	RO	LMTIMS LAN MAC Transmit Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Interrupt is enabled and its corresponding status bit is set.
16	0	RO	LMRIMS LAN MAC Receive Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Interrupt is enabled and its corresponding status bit is set.
15	0	RO	LMTBUMS LAN MAC Transmit Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
14	0	RO	LMRBUMS LAN MAC Receive Buffer Unavailable Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt is enabled and its corresponding status bit is set.
13	0	RO	LMTPSMS LAN MAC Transmit Process Stopped Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt is enabled and its corresponding status bit is set.
12	0	RO	LMRPSMS LAN MAC Receive Process Stopped Interrupt Mask Status When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt is enabled and its corresponding status bit is set.
11	0	RO	MSIMS Modem Status Interrupt Mask Status When this bit is set, it indicates that the Modem status Interrupt is enabled and its corresponding status bit is set.
10	0	RO	ULEIMS UART Line Error Interrupt Mask Status When this bit is set, it indicates that the UART Line Error Status Interrupt is enabled and its corresponding status bit is set. UART line error status is defined as logic OR of the following line conditions: Overrun Error, parity error, framing error, break interrupt.
9	0	RO	URIMS UART Receive Interrupt Mask Status When this bit is set, it indicates that the UART receive interrupt is enabled and its corresponding status bit is set.
8	0	RO	UTIMS UART Transmit Interrupt Mask Status When this bit is set, it indicates that the UART transmit interrupt is enabled and its corresponding status bit is set.
7	0	RO	TIIMS Timer 1 Interrupt Mask Status When this bit is set, it indicates that the Timer 1 Interrupt is enabled and its corresponding status bit is set.
6	0	RO	TOIMS Timer 0 Interrupt Mask Status



			When this bit is set, it indicates that the Timer 0 Interrupt is enabled and its corresponding status bit is set.
5	0	RO	EXTI3MS External Interrupt 3 Mask Status When this bit is set, it indicates that the external interrupt 3 is enabled and its corresponding status bit is set.
4	0	RO	EXTI2MS External Interrupt 2 Mask Status When this bit is set, it indicates that the external interrupt 2 is enabled and its corresponding status bit is set.
3	0	RO	EXTI1MS External Interrupt 1 Mask Status When this bit is set, it indicates that the external interrupt 1 is enabled and its corresponding status bit is set.
2	0	RO	EXTI0MS External Interrupt 0 Mask Status When this bit is set, it indicates that the external interrupt 0 is enabled and its corresponding status bit is set.
1	0	RO	CCTMS Communications Channel Transmit Mask Status When this bit is set, it indicates that the Communications Channel Transmit is enabled and its corresponding status bit is set..
0	0	RO	CCRMS Communications Channel Receive Mask Status When this bit is set, it indicates that the Communications Channel Receive is enabled and its corresponding status bit is set..

### 3.6.12 Interrupt Pending Highest Priority Register for FIQ (INTHPF Offset 0xE230)

This register provides the interrupt information for the host to identify the pending interrupts with highest priority for FIQ (fast interrupt). Note that it is possible to have more than one highest interrupts pending because of the same priority level. This register is provided to the host to quickly identify and service the FIQ interrupt with highest priority. This register is read only.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIPF WAN MAC Link Changed Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Link Changed Interrupt has the highest priority among all the FIQ interrupts pending currently.
30	0	RO	WMTIPF WAN MAC Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Interrupt has the highest priority among all the FIQ interrupts pending currently.
29	0	RO	WMRIPF WAN MAC Receive Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Interrupt has the highest priority among all the FIQ interrupts pending currently.
28	0	RO	WMTBUIPF WAN MAC Transmit Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
27	0	RO	WMRBUIPF WAN MAC Receive Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
26	0	RO	WMTSPIPF WAN MAC Transmit Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt

			has the highest priority among all the FIQ interrupts pending currently.
25	0	RO	WMRPSIPF WAN MAC Receive Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
24	0	RO	ABERPF AMBA Bus Error Response Interrupt Pending for FIQ When this bit is set, it indicates that the AMBA Bus Error Response Interrupt has the highest priority among all the FIQ interrupts pending currently.
23	0	RO	Reserved. For factory test purpose only.
22	0	RO	Reserved. For factory test purpose only.
21	0	RO	Reserved. For factory test purpose only.
20	0	RO	Reserved. For factory test purpose only.
19	0	RO	Reserved. For factory test purpose only.
18	0	RO	Reserved. For factory test purpose only.
17	0	RO	LMTIPF LAN MAC Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Interrupt has the highest priority among all the FIQ interrupts pending currently.
16	0	RO	LMRIPF LAN MAC Receive Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Receive Interrupt has the highest priority among all the FIQ interrupts pending currently.
15	0	RO	LMTBUIPF LAN MAC Transmit Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
14	0	RO	LMRBUIPF LAN MAC Receive Buffer Unavailable Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the FIQ interrupts pending currently.
13	0	RO	LMTPSIPF LAN MAC Transmit Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
12	0	RO	LMRPSIPF LAN MAC Receive Process Stopped Interrupt Pending for FIQ When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt has the highest priority among all the FIQ interrupts pending currently.
11	0	RO	MSIPF Modem Status Interrupt Pending for FIQ When this bit is set, it indicates that the Modem status Interrupt has the highest priority among all the FIQ interrupts pending currently.
10	0	RO	ULEIPF UART Line Error Interrupt Pending for FIQ When this bit is set, it indicates that the UART Line Error Status Interrupt has the highest priority among all the FIQ interrupts pending currently.
9	0	RO	URIPF UART Receive Interrupt Pending for FIQ When this bit is set, it indicates that the UART receive interrupt has the highest priority among all the FIQ interrupts pending currently.
8	0	RO	UTIPF UART Transmit Interrupt Pending for FIQ When this bit is set, it indicates that the UART transmit interrupt has the highest priority among all the FIQ interrupts pending currently.
7	0	RO	T1IPF Timer 1 Interrupt Pending for FIQ When this bit is set, it indicates that the Timer 1 Interrupt has the highest priority among all the FIQ interrupts pending currently.
6	0	RO	T0IPF Timer 0 Interrupt Pending for FIQ When this bit is set, it indicates that the Timer 0 Interrupt has the highest priority among

			all the FIQ interrupts pending currently.
5	0	RO	EXTI3PF External Interrupt 3 Pending for FIQ When this bit is set, it indicates that the external interrupt 3 has the highest priority among all the FIQ interrupts pending currently.
4	0	RO	EXTI2PF External Interrupt 2 Pending for FIQ When this bit is set, it indicates that the external interrupt 2 has the highest priority among all the FIQ interrupts pending currently.
3	0	RO	EXTI1PF External Interrupt 1 Pending for FIQ When this bit is set, it indicates that the external interrupt 1 has the highest priority among all the FIQ interrupts pending currently.
2	0	RO	EXTI0PF External Interrupt 0 Pending for FIQ When this bit is set, it indicates that the external interrupt 0 has the highest priority among all the FIQ interrupts pending currently.
1	0	RO	CCTPF Communications Channel Transmit Pending for FIQ When this bit is set, it indicates that the Communications Channel Transmit has the highest priority among all the FIQ interrupts pending currently..
0	0	RO	CCRPF Communications Channel Receive Pending for FIQ When this bit is set, it indicates that the Communications Channel Receive has the highest priority among all the FIQ interrupts pending currently..

### 3.6.13 Interrupt Pending Highest Priority Register for IRQ (INTHPI Offset 0xE234)

This register provides the interrupt information for the host to identify the pending interrupts with highest priority for IRQ (normal interrupt) Note that it is possible to have more than one highest interrupts pending because of the same priority level. This register is provided to the host to quickly identify and service the IRQ interrupt with the highest priority. This register is read only.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	WMLCIPQ WAN MAC Link Changed Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Link Changed Interrupt has the highest priority among all the IRQ interrupts pending currently.
30	0	RO	WMTIPQ WAN MAC Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Transmit Interrupt has the highest priority among all the IRQ interrupts pending currently.
29	0	RO	WMRIPQ WAN MAC Receive Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Interrupt has the highest priority among all the IRQ interrupts pending currently.
28	0	RO	WMTBUIPQ WAN MAC Transmit Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
27	0	RO	WMRBUIPQ WAN MAC Receive Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
26	0	RO	WMTSPIPQ WAN MAC Transmit Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Transmit Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.

25	0	RO	WMRPSIPQ WAN MAC Receive Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the WAN MAC Receive Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
24	0	RO	ABERPF AMBA Bus Error Response Interrupt Pending for IRQ When this bit is set, it indicates that the AMBA Bus Error Response Interrupt has the highest priority among all the IRQ interrupts pending currently.
23	0	RO	Reserved. For factory test purpose only.
22	0	RO	Reserved. For factory test purpose only.
21	0	RO	Reserved. For factory test purpose only.
20	0	RO	Reserved. For factory test purpose only.
19	0	RO	Reserved. For factory test purpose only.
18	0	RO	Reserved. For factory test purpose only.
17	0	RO	LMTIPQ LAN MAC Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Interrupt has the highest priority among all the IRQ interrupts pending currently.
16	0	RO	LMRIPQ LAN MAC Receive Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Interrupt has the highest priority among all the IRQ interrupts pending currently.
15	0	RO	LMTBUIPQ LAN MAC Transmit Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
14	0	RO	LMRBUIPQ LAN MAC Receive Buffer Unavailable Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Buffer Unavailable Interrupt has the highest priority among all the IRQ interrupts pending currently.
13	0	RO	LMTPSIPQ LAN MAC Transmit Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Transmit Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
12	0	RO	LMRPSIPQ LAN MAC Receive Process Stopped Interrupt Pending for IRQ When this bit is set, it indicates that the LAN MAC Receive Process Stopped Interrupt has the highest priority among all the IRQ interrupts pending currently.
11	0	RO	MSIPQ Modem Status Interrupt Pending for IRQ When this bit is set, it indicates that the Modem status Interrupt has the highest priority among all the IRQ interrupts pending currently.
10	0	RO	ULEIPQ UART Line Error Interrupt Pending for IRQ When this bit is set, it indicates that the UART Line Error Status Interrupt has the highest priority among all the IRQ interrupts pending currently.
9	0	RO	URIPQ UART Receive Interrupt Pending for IRQ When this bit is set, it indicates that the UART receive interrupt has the highest priority among all the IRQ interrupts pending currently.
8	0	RO	UTIPQ UART Transmit Interrupt Pending for IRQ When this bit is set, it indicates that the UART transmit interrupt has the highest priority among all the IRQ interrupts pending currently.
7	0	RO	T1IPQ Timer 1 Interrupt Pending for IRQ When this bit is set, it indicates that the Timer 1 Interrupt has the highest priority among all the IRQ interrupts pending currently.
6	0	RW	T0IPQ Timer 0 Interrupt Pending for IRQ When this bit is set, it indicates that the Timer 0 Interrupt has the highest priority among all the IRQ interrupts pending currently.

5	0	RO	EXTI3PQ External Interrupt 3 Pending for IRQ When this bit is set, it indicates that the external interrupt 3 has the highest priority among all the IRQ interrupts pending currently.
4	0	RO	EXTI2PQ External Interrupt 2 Pending for IRQ When this bit is set, it indicates that the external interrupt 2 has the highest priority among all the IRQ interrupts pending currently.
3	0	RO	EXTI1PQ External Interrupt 1 Pending for IRQ When this bit is set, it indicates that the external interrupt 1 has the highest priority among all the IRQ interrupts pending currently.
2	0	RO	EXTI0PQ External Interrupt 0 Pending for IRQ When this bit is set, it indicates that the external interrupt 0 has the highest priority among all the IRQ interrupts pending currently.
1	0	RO	CCTPQ Communications Channel Transmit Pending for IRQ When this bit is set, it indicates that the Communications Channel Transmit has the highest priority among all the IRQ interrupts pending currently.
0	0	RO	CCRPQ Communications Channel Receive Pending for IRQ When this bit is set, it indicates that the Communications Channel Receive has the highest priority among all the IRQ interrupts pending currently..

## 3.7 Timer Registers

### 3.7.1 Timer Control Register (TMCON Offset 0xE400)

The KS8695X has two 32-bit timers(Timer 0 and Timer 1). When the timer expires, it generates a pulse on the I/O pins. These timer can operate in a very flexible way. The host can control the timeout period as well as the pulse duration. The output signals are TOUT1 and TOUT0, respectively. These timers are enabled or disabled by this register. Interrupt can be generated by setting the corresponding interrupt control registers.

A timer generates a one-shot pulse with a preset timer clock duration whenever a timeout occurs. The duration of the one-shot pulse is also programmable by the host. This pulse consequently generates a time-out interrupt that is directly observable at the timers's configured output pin. The timer frequency is calculated as follows:

$$f_{TOUT} = f_{MCLK} / ((\text{Timer data value} + \text{Pulse data value}))$$

When the timer is enabled, it loads a data value to its count register and begins decrementing the count register value. When the timer expires, the corresponding TOUT pin is then asserted. Then it loads the pulse count value into the count register and starts decrementing. When the pulse data count reaches zero, the associated interrupt is asserted ( if enabled ), the TOUT pin is deasserted, and the timer data value is reloaded again for the next timeout. This process repeats until the timer is disabled. In our design, the frequency of MCLK is 25MHz.

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:2	0	RO	Reserved
1	0	RW	TOUT1E Timer 1 Enable When set, the timer 1 is enabled. Timer process starts as soon as this bit is set. Software should ensure correct timer count and pulse data values are preloaded before setting this bit.
0	0	RW	TOUT0E Timer 0 Enable



			When set, the timer 0 is enabled. Timer process starts as soon as this bit is set. Software should ensure correct timer count and pulse data values are preloaded before setting this bit.
--	--	--	--

### 3.7.2 Timer 1 Timeout Count Register (T1TC Offset 0xE404)

This register controls the timeout count value to be preloaded to the down-counting register for Timer 1. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	TOUT1TC Timer 1 Timeout Count This field specifies the duration that the TOUT1 pin is Low in each timeout period. Writing zero to this register may cause unpredictable behavior.

### 3.7.3 Timer 0 Timeout Count Register (T0TC Offset 0xE408)

This register controls the timeout count value to be preloaded to the down-counting register for Timer 0. Writing a zero to this register may result in unpredictable timer behavior.

Timer 0 can also be programmed as Watchdog timer when the Byte 0 of Timeout Count Register is programmed as 8'hFF. Once it has been programmed as a Watchdog timer, the value in Timeout Count Register can never be re-programmed unless the timer is disabled first. In normal system operation, the Watchdog timer will be periodically disabled by CPU before it expires. In case the Watchdog timer expires (indicating system gets hung and CPU can not periodically come in to clear the timer by clearing the timer enable bit), a reset signal (active high) will be generated to reset the whole system.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	ffff_ff00	RW	TOUT0TC Timer 0 Timeout Count This field specifies the duration that the TOUT0 pin is Low in each timeout period. Writing zero to this register may cause unpredictable behavior. Note that if the lowest byte is configured as 8'hFF, Timer 0 becomes Watchdog Timer.

### 3.7.4 Timer 1 Pulse Count Register (T1PD Offset 0xE40C)

This register controls the pulse data value to be preloaded to the down-counting register for Timer 1. The TOUT1 pin output remains asserted at '1' until the pulse counter reaches zero. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	TOUT1PC Timer 1 Pulse Count This field specifies the duration that the TOUT1 pin is High in each timeout period. Writing zero to this register may cause unpredictable behavior.

### 3.7.5 Timer 0 Pulse Count Register (T0PD Offset 0xE410)

This register controls the pulse data value to be preloaded to the down-counting register for Timer 0. The TOUT0 pin output remains asserted at '1' until the pulse counter reaches zero. Writing a zero to this register may result in unpredictable timer behavior.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	--	RW	TOUT0PC Timer 0 Pulse Count This field specifies the duration that the TOUT0 pin is High in each timeout period. Writing zero to this register may cause unpredictable behavior.

## 3.8 GPIO Registers

### 3.8.1 I/O Port Mode Register (IOPM Offset 0xE600)

This register controls the I/O pin input output mode. Each I/O pin can be configured as Input or Output. Note that some of the I/O pins are shared with the external interrupts and timer output. When these pins are configured for timer output, it overrides the I/O Port Mode configuration. If the pins shared with External Interrupt (GPIO pins 3 to 0) are configured as output pins and are enabled for External/Soft Interrupt (e.g. Port Control Register bit 15 is set to 1 enable the External/Soft Interrupt 3), CPU can generate a soft interrupt by writing appropriate data (based on Trigger Mode defined in Port Control Register) to the corresponding Port Data Register.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7	0	RW	IOPM7 I/O Port Mode for GPIO Pin 7 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
6	0	RW	IOPM6 I/O Port Mode for GPIO Pin 6 When set, the port is configured as an output pin. When reset, the port is configured as an input pin.
5	0	RW	IOPM5 I/O Port Mode for GPIO Pin 5 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 5 is shared with Timer 1 output.
4	0	RW	IOPM4 I/O Port Mode for GPIO Pin 4 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 4 is shared with Timer 0 output.
3	0	RW	IOPM3 I/O Port Mode for GPIO Pin 3 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 3 is shared with External Interrupt 3 input.
2	0	RW	IOPM2 I/O Port Mode for GPIO Pin 2 When set, the port is configured as an output pin.



			When reset, the port is configured as an input pin. Note that GPIO Pin 2 is shared with External Interrupt 2 input.
1	0	RW	IOPM1 I/O Port Mode for GPIO Pin 1 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 1 is shared with External Interrupt 1 input.
0	0	RW	IOPM0 I/O Port Mode for GPIO Pin 0 When set, the port is configured as an output pin. When reset, the port is configured as an input pin. Note that GPIO Pin 0 is shared with External Interrupt 0 input.

### 3.8.2 I/O Port Control Register (IOPC Offset 0xE604)

This register controls the usage of the shared I/O pins.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:18	0	RO	Reserved
17	0	RW	IOTIM1EN GPIO Pin for Timer 1 Enable When set, the shared GPIO pin (TOUT1) for Timer 1 is used for the timer. When reset, the shared GPIO pin for Timer 1 is used for normal GPIO purpose.
16	0	RW	IOTIM0EN GPIO Pin for Timer 0 Enable When set, the shared GPIO pin (TOUT0) for Timer 0 is used for the timer. When reset, the shared GPIO pin for Timer 0 is used for normal GPIO operation.
15	0	RW	IOEINT3EN GPIO Pin for External/Soft Interrupt 3 Enable When set, the shared GPIO pin (EXT3) for external interrupt request 3 is used for the interrupt. When reset, the shared GPIO pin (EXT3) for external interrupt request 3 is used for normal GPIO operation.
14:12	0	RW	IOEINT3TM GPIO Pin for External/Soft Interrupt 3 Trigger Mode This field is used to configure the trigger mode for External Interrupt 3. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection
11	0	RW	IOEINT2EN GPIO Pin for External/Soft Interrupt 2 Enable When set, the shared GPIO pin (EXT2) for external interrupt request 2 is used for the interrupt. When reset, the shared GPIO pin (EXT2) for external interrupt request 2 is used for normal GPIO operation.
10:8	0	RW	IOEINT2TM GPIO Pin for External/Soft Interrupt 2 Trigger Mode This field is used to configure the trigger mode for External Interrupt 2. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection

			10x= Falling Edge Detection 11x= Both Edge Detection
7	0	RW	IOEINT1EN GPIO Pin for External/Soft Interrupt 1 Enable When set, the shared GPIO pin (EXT1) for external interrupt request 1 is used for the interrupt. When reset, the shared GPIO pin (EXT1) for external interrupt request 1 is used for normal GPIO operation.
6:4	0	RW	IOEINT1TM GPIO Pin for External/Soft Interrupt 1 Trigger Mode This field is used to configure the trigger mode for External Interrupt 1. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection
3	0	RW	IOEINT0EN GPIO Pin for External/Soft Interrupt 0 Enable When set, the shared GPIO pin (EXT0) for external interrupt request 0 is used for the interrupt. When reset, the shared GPIO pin (EXT0) for external interrupt request 0 is used for normal GPIO operation.
2:0	0	RW	IOEINT0TM GPIO Pin for External/Soft Interrupt 0 Trigger Mode This field is used to configure the trigger mode for External Interrupt 0. 000= Level Detection (Active Low) 001= Level Detection (Active High) 01x= Rising Edge Detection 10x= Falling Edge Detection 11x= Both Edge Detection

### 3.8.3 I/O Port Data Register (IOPD Offset 0xE608)

This register contains the one-bit read values for I/O ports that are configured as input port, and one-bit write value for I/O ports that are configured as output port. Bits[7:0] of the 8-bit I/O port register value correspond directly to the 8 I/O pins, GPIO[7:0].

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:0	--	RW	IOPD I/O Port Data Value The values reflect the signal level on the respective I/O port pins. When the ports are configured as output port, the bit reflects the port write value. When the port is configured as input port, the bit reflects the port read value.

## 3.9 Switch Engine Registers

Note 1: unless otherwise specified,

1 = feature enabled,

0 = feature disabled

Note 2: BIST procedure:

Hold hardware reset active and hold BIST = 0, wait for 1000ns, change BIST = 1

Note 3: To ensure no dropped packets in half duplex mode, 0xE800, bit 5 must be set to '1'. This is not set by default because it is not the IEEE standard.

### 3.9.1 Switch Engine Control 0 Register (SEC0 Offset 0xE800)

Note: Flow control fair mode bit (12) is used in situations where not all port partners have flow control ability. In these cases, when the output port queue reaches the high water mark, packets coming from ports without flow control will be dropped. The ports with flow control will still continue to function normally. When it drops below the low water mark, packets from the ports without flow control will no longer be dropped.

The following table shows the register bit fields. Default: 0x4FE6\_B780

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	New back off algorithm to meet UNH requirement
30:28	0x4	RW	Used as 802.1p user priority comparison base. If greater than or equal to this value, the 802.1p packet will be classified as high priority.
27:25	0	RW	LLED1S LAN LED1 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
24:22	0x6	RW	LLED0S LAN LED0 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
21	1	RW	New flow control compliance fix for UNH, respond to unicast flow control.
20	0	RW	Automatic fast age when link change detected.
19	0	RW	Pass all error packets (debug purpose).
18	1	RW	Enable "port 5" flow control
17	1	RW	Enable flow control function for ports 1-4. The final flow control depends on the auto negotiation results.
16	0	RW	Buffer share mode
15	1	RW	Aging enable
14	0	RW	Enable fast aging by software
13	1	RW	Fast back off mode
12	1	RW	Port based vlan mismatch discard. 0, will allow unicast packets cross VLAN boundary
11	0	RW	Don't apply broadcast storm protection to multicast packets.

10	1	RW	Backpressure mode. 1, preamble based 0, collision based
9	1	RW	Flow control fair mode. 1, fair mode enable 0, no fair mode
8	1	RW	No excessive collision drop ( $\geq 16$ ).
7	1	RW	Enforce max length check (1518 or 1522) 0, allow to receive 1536
6	0	RW	6K Byte buffer per port reserved for high priority packets.
5	0	RW	Backpressure enable. Must be turned on to prevent packet loss in half duplex mode.
4	0		Reserved
3:2	0x0	RW	Priority scheme: 00, always transmit high 01, 10:1 for high/low ratio 10, 5:1 for high/low ratio 11, 2:1 for high/low ratio
1	0	RW	Tag special mode (use tag to define mask to send packet).
0	0	RW	Enable switch function. 1, switch enabled to receive and transmit. 0, no packets will be received or transmitted

### 3.9.2 Switch Engine Control 1 Register (SEC1 Offset 0xE804)

The following table shows the register bit fields. Default: 0xE824\_2824

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0xE8	RW	Broadcast Storm Protection Rate. These bits determine how many “64 byte” units of packet data are allowed on an input port in a preset period. 50ms for 100BT or 500ms for 10BT. The rate can be set in increments of 8 “64 byte” units.
23:0	0x242824	RO	Factory default. Do not change.

### 3.9.3 Port 1 Configuration Register (SEP1C Offset 0xE808)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Tag value for the port (ingress).
15	0	RW	Disable auto negotiation.
14	0	RW	Forced 100 when auto negotiation is disabled.
13	0	RW	Forced full duplex when auto negotiation is disabled.
12:8	0x1F	RW	Specify ports that port 1 can talk to (port VLAN).
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded.
5	0	RW	Spanning Tree learning disable on the port.
4	0	RW	Broadcast Storm protection on the port.

3	0	RW	High priority on the port (ingress).
2	0	RW	Enable TOS based priority classification on the port (ingress).
1	0	RW	Enable 802.1p based priority classification on the port (ingress)
0	0	RW	Enable priority function on the port (egress)

### 3.9.4 Port 2 Configuration Register (SEP2C Offset 0x E80C)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Tag value for the port (ingress).
15	0	RW	Disable auto negotiation.
14	0	RW	Forced 100 when auto negotiation is disabled.
13	0	RW	Forced full duplex when auto negotiation is disabled.
12:8	0x1F	RW	Specify ports that port 2 can talk to (port VLAN).
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded.
5	0	RW	Spanning Tree learning disable on the port.
4	0	RW	Broadcast Storm protection on the port.
3	0	RW	High priority on the port (ingress).
2	0	RW	Enable TOS based priority classification on the port (ingress).
1	0	RW	Enable 802.1p based priority classification on the port (ingress)
0	0	RW	Enable priority function on the port (egress)

### 3.9.5 Port 3 Configuration Register (SEP3C Offset 0xE810)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Tag value for the port (ingress).
15	0	RW	Disable auto negotiation.
14	0	RW	Forced 100 when auto negotiation is disabled.
13	0	RW	Forced full duplex when auto negotiation is disabled.
12:8	0x1F	RW	Specify ports that port 3 can talk to (port VLAN).
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded.
5	0	RW	Spanning Tree learning disable on the port.
4	0	RW	Broadcast Storm protection on the port.
3	0	RW	High priority on the port (ingress).
2	0	RW	Enable TOS based priority classification on the port (ingress).
1	0	RW	Enable 802.1p based priority classification on the port (ingress)
0	0	RW	Enable priority function on the port (egress)

### 3.9.6 Port 4 Configuration Register (SEP4C Offset 0xE814)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Tag value for the port (ingress).
15	0	RW	Disable auto negotiation.
14	0	RW	Forced 100 when auto negotiation is disabled.
13	0	RW	Forced full duplex when auto negotiation is disabled.
12:8	0x1F	RW	Specify ports that port 4 can talk to (port VLAN).
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded.
5	0	RW	Spanning Tree learning disable on the port.
4	0	RW	Broadcast Storm protection on the port.
3	0	RW	High priority on the port (ingress).
2	0	RW	Enable TOS based priority classification on the port (ingress).
1	0	RW	Enable 802.1p based priority classification on the port (ingress)
0	0	RW	Enable priority function on the port (egress)

### 3.9.7 Port 5 Configuration Register (SEP5C Offset 0xE818)

The following table shows the register bit fields. Default: 0x0000\_1FC0

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0000	RW	Tag value for the port (ingress).
15	0		Reserved
14	0	RW	Receive direct mode.
13	0	RW	Transmit pre-tag mode.
12:8	0x1F	RW	Specify ports that port 5 can talk to (port VLAN).
7	1	RW	Spanning Tree transmit enable on the port, BPDU excluded.
6	1	RW	Spanning Tree receive enable on the port, BPDU excluded.
5	0	RW	Spanning Tree learning disable on the port.
4	0	RW	Broadcast Storm protection on the port.
3	0	RW	High priority on the port (ingress).
2	0	RW	Enable TOS based priority classification on the port (ingress).
1	0	RW	Enable 802.1p based priority classification on the port (ingress)
0	0	RW	Enable priority function on the port (egress)

### 3.9.8 Ports 1 & 2 Auto Negotiation (AN) Register (SEP12AN Offset 0xE81C)

The following table shows the register bit fields. Default: 0x1F00\_1F00

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0		Reserved
30	0	RO	Port 1 AN complete.

29	0	RW	Port 1 AN restart.
28	1	RW	Port 1 AN advertise pause.
27	1	RW	Port 1 AN advertise 100 Full Duplex.
26	1	RW	Port 1 AN advertise 100 Half Duplex.
25	1	RW	Port 1 AN advertise 10 Full Duplex.
24	1	RW	Port 1 AN advertise 10 Half Duplex.
23	0	RO	Port 1 Link status.
22	0	RO	Port 1 duplex status (resolved).
21	0	RO	Port 1 speed status (resolved).
20	0	RO	Port 1 Link Partner pause.
19	0	RO	Port 1 Link Partner 100 Full Duplex.
18	0	RO	Port 1 Link Partner 100 Half Duplex.
17	0	RO	Port 1 Link Partner 10 Full Duplex.
16	0	RO	Port 1 Link Partner 10 Half Duplex.
15	0		Reserved
14	0	RO	Port 2 AN complete.
13	0	RW	Port 2 AN restart.
12	1	RW	Port 2 AN advertise pause.
11	1	RW	Port 2 AN advertise 100 Full Duplex.
10	1	RW	Port 2 AN advertise 100 Half Duplex.
9	1	RW	Port 2 AN advertise 10 Full Duplex.
8	1	RW	Port 2 AN advertise 10 Half Duplex.
7	0	RO	Port 2 Link status.
6	0	RO	Port 2 duplex status (resolved).
5	0	RO	Port 2 speed status (resolved).
4	0	RO	Port 2 Link Partner pause.
3	0	RO	Port 2 Link Partner 100 Full Duplex.
2	0	RO	Port 2 Link Partner 100 Half Duplex.
1	0	RO	Port 2 Link Partner 10 Full Duplex.
0	0	RO	Port 2 Link Partner 10 Half Duplex.

### 3.9.9 Ports 3 & 4 Auto Negotiation (AN) Register (SEP34AN Offset 0xE820)

The following table shows the register bit fields. Default: 0x1F00\_1F00

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0		Reserved
30	0	RO	Port 3 AN complete.
29	0	RW	Port 3 AN restart.
28	1	RW	Port 3 AN advertise pause.
27	1	RW	Port 3 AN advertise 100 Full Duplex.
26	1	RW	Port 3 AN advertise 100 Half Duplex.
25	1	RW	Port 3 AN advertise 10 Full Duplex.
24	1	RW	Port 3 AN advertise 10 Half Duplex.



23	0	RO	Port 3 Link status.
22	0	RO	Port 3 duplex status (resolved).
21	0	RO	Port 3 speed status (resolved).
20	0	RO	Port 3 Link Partner pause.
19	0	RO	Port 3 Link Partner 100 Full Duplex.
18	0	RO	Port 3 Link Partner 100 Half Duplex.
17	0	RO	Port 3 Link Partner 10 Full Duplex.
16	0	RO	Port 3 Link Partner 10 Half Duplex.
15	0		Reserved
14	0	RO	Port 4 AN complete.
13	0	RW	Port 4 AN restart.
12	1	RW	Port 4 AN advertise pause.
11	1	RW	Port 4 AN advertise 100 Full Duplex.
10	1	RW	Port 4 AN advertise 100 Half Duplex.
9	1	RW	Port 4 AN advertise 10 Full Duplex.
8	1	RW	Port 4 AN advertise 10 Half Duplex.
7	0	RO	Port 4 Link status.
6	0	RO	Port 4 duplex status (resolved).
5	0	RO	Port 4 speed status (resolved).
4	0	RO	Port 4 Link Partner pause.
3	0	RO	Port 4 Link Partner 100 Full Duplex.
2	0	RO	Port 4 Link Partner 100 Half Duplex.
1	0	RO	Port 4 Link Partner 10 Full Duplex.
0	0	RO	Port 4 Link Partner 10 Half Duplex.

### 3.9.10 Look-up Engine (LUE) Control Register (SELUEC Offset 0xE824)

The following table shows the register bit fields.

Note: a write will trigger a LUE command.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:13	0x00000	RO	Reserved
12	0	RO	Command busy: 1, will not accept new command. 0, can accept new command
11	0	WO	Command read/write (self clearing): 1, read command 0, write command
10	0	RW	Table select: 1, Dynamic Table 0, Static Table
9:0	0x000	RW	Address within the selected table (dynamic or static).

### 3.9.11 Look-up Engine (LUE) Indirect Register High (SELUEIH Offset 0xE828)

The following table shows the register bit fields.

Note: it is indirect, so the value written may not equal the value read.

Static Table Selected

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:23	0x0		Reserved
22	0	RW	LUE override, used for BPDU packets to override txen=0 or rxen=0
21	0	RW	Valid: 1-> entry is valid, 0 -> entry is not valid
20:16	-	RW	Port location: Bit 16: 1 -> Port 1 selected, 0 -> Port 1 not selected Bit 17: 1 -> Port 2 selected, 0 -> Port 2 not selected Bit 18: 1 -> Port 3 selected, 0 -> Port 3 not selected Bit 19: 1 -> Port 4 selected, 0 -> Port 4 not selected Bit 20: 1 -> internal LAN DMA port selected, 0 -> internal LAN DMA port not selected
15:0	-	RW	MAC address [47:32]

Dynamic Table Selected

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	-	RO	MAC table empty status: 1 -> empty, 0 -> not empty
30:21	-	RO	Number of entries: 0 -> 1 entry, 3FF -> 1K entries
20:19	-	RO	Time stamp
18:16	-	RO	Port location (encoded): 000 -> Port 1 001 -> Port 2 010 -> Port 3 011 -> Port 4 100 -> internal LAN DMA port
15:0	-	RO	MAC address [47:32]

### 3.9.12 Look-up Engine (LUE) Indirect Register Low (SELUEIL Offset 0xE82C)

The following table shows the register bit fields. Default: 0x0000\_0000

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	-	RW	MAC address [31:0]

Application note :

For consecutive LUE commands, check that SELUEC bit 12 is cleared before issuing the next LUE command. Always wait 200 ns between each consecutive read of the SELUE registers: SELUEC, SELUEIH, and SELUEIL.

For static table writes, write to SELUEIH and SELUEIL first and then write to SELUEC with bits [11:10] = 00.

For static table reads, write to SELUEC with bits [11:10] = 10, wait 200 ns, continuously check SELUEC bit 12 until it is cleared. When SELUEC bit 12 is cleared, read SELUEIH, wait 200 ns, and then read SELUEIL.

For dynamic table reads, write to SELUEC with bits [11:10] = 11, wait 200 ns, continuously check SELUEC bit 12 until it is cleared. When SELUEC bit 12 is cleared, read SELUEIH, wait 200 ns, and then read SELUEIL.

Static Table format [54:0]:

- bit 54: LUE override, used for BPDU packets to override txen=0 or rxen=0
- bit 53: valid
- bit 52-48: port map
- bit 47-0: mac address

Dynamic Table format [63:0]:

- bit 63: MAC table empty
- bit 62-53 : number of entries
- bit 52-51: time stamp
- bit 50-48: port location (encoded)
- bit 47-0: MAC address

## 3.9.13 Advance Feature Control Register (SEAF C Offset 0xE830)

The following table shows the register bit fields. Default: 0x0000\_0000

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:27	0x00		Reserved
26:22	0x00	RW	Tag removal (msb = port 5, lsb= port 1) Bit 26, tag removal for internal LAN DMA port Bit 25, tag removal for port 4 Bit 24, tag removal for port 3 Bit 23, tag removal for port 2 Bit 22, tag removal for port 1
21:17	0x00	RW	Tag insertion (msb = port 5, lsb= port 1) Bit 21, tag insertion for internal LAN DMA port Bit 20, tag insertion for port 4 Bit 19, tag insertion for port 3 Bit 18, tag insertion for port 2 Bit 17, tag insertion for port 1
16	0	RW	Sniffer mode: 1, AND – sniffer port will only look at packets that are received on the RX mirror port AND transmitted out from the TX mirror port 0, OR – sniffer port will look at packets that are received on the RX mirror port OR transmitted from the TX mirror port.
15:11	0x00	RW	Sniffer port select (msb = port 5, lsb= port 1) Bit 15, select internal LAN DMA port as sniffer port Bit 14, select port 4 as sniffer port Bit 13, select port 3 as sniffer port Bit 12, select port 2 as sniffer port Bit 11, select port 1 as sniffer port
10:6	0x00	RW	TX mirror port select (msb = port 5, lsb= port 1) 10, select internal LAN DMA port as TX mirror port

			9, select port 4 as TX mirror port 8, select port 3 as TX mirror port 7, select port 2 as TX mirror port 6, select port 1 as TX mirror port
5:1	0x00	RW	RX mirror port select (msb = port 5, lsb= port 1) 5, select internal LAN DMA port as RX mirror port 4, select port 4 as RX mirror port 3, select port 3 as RX mirror port 2, select port 2 as RX mirror port 1, select port 1 as RX mirror port
0	0	RW	IGMP trap enable (trapped to internal LAN DMA port)

### 3.9.14 DSCP Register High (SEDSCPH Offset 0xE834)

Note: Differentiated Services Code Point (DSCP) is a fully decoded 64 bit register used to determine priority from DSCP field (6 bits) in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is compared against the corresponding bit in the DSCP register. If the register bit is a 1, the priority is high; and if 0, the priority is low.

The following table shows the register bit fields. Default: 0x0000\_0000

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	DSCP [63:32]

### 3.9.15 DSCP Register Low (SEDSCPL Offset 0xE838)

The following table shows the register bit fields. Default: 0x0000\_0000

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0x0	RW	DSCP [31:0]

### 3.9.16 Switch Engine MAC Address Register High (SEMAH Offset 0xE83C)

The following table shows the register bit fields. Default: 0x0000\_0010

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0x0		Reserved
15:0	0x0010	RW	MAC address [47:32]

### 3.9.17 Switch Engine MAC Address Register Low (SEMAL Offset 0xE840)

The following table shows the register bit fields. Default: 0xA1FF\_FFFF

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:0	0xA1FF_FFFF	RW	MAC address [31:0]

### 3.9.18 Management Counter Indirect Access Register (SEMCIA Offset 0xE844)

The following table shows the register bit fields. Default: 0x0000\_0000

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	-		Reserved.
7:0	0x00	RW	Counter Address

### 3.9.19 Management Counter Data Register (SEMCD Offset 0xE848)

The following table shows the register bit fields.

Note: the access sequence is to set register SEMCIA first, and then read SEMCD. If bit 31 is not 1, continue to read until that bit is a 1, meaning counter value [29:0] is valid. If bit 30 is a 1, overflow has occurred. Do a dummy write to SEMCD to clear bit 30.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RO	Counter value [29:0] is valid
30	0	RO	Counter has wrapped around (overflow)
29:0	-	RO	Counter value

Register Definition:

QM Counters (2)

txdrop: Transmit drop due to lack of resources, number of packets

rxdrop: Receive drop due to lack of resources, number of packets

RX Counters (20)

Rxbyte: Receive octet count including bad packets (RMON, MIB2), note Etherlike requires no MAC control frame. This can be achieved by deducting the number of MAC control frames \* 64.

Rxudsz: Receive undersize, good CRC

Rxfrgm: Receive fragment, bad CRC

Rxovsz: Receive oversize, good CRC (max 1536)

Rxjabr: Receive jabber, bad CRC

Rxmmer: Receive coding error

Rxcrc: Receive CRC error

Rxalgn: Receive alignment error

Rxmacf: Receive good MAC control frames (check 8808)

Rxmacp: Receive good MAC control frames (check DA (uni/broadcast) and 8808 and op code)

Rxbcast: Receive good broadcast frame count

Rxmcast: Receive good multicast frame count, excluding MAC control frames and excluding broadcast frames.

Rxucast: Receive good unicast, excluding MAC control (RMON does not specify)

	<64	>Max (64, max)	crcer	mmer	nibble	ctrl
rxudsz	Y		N	N		
rxfrgm	Y		Y or	Y		
rxovsz		Y	N	N		
rxjabr		Y	Y or	Y		
rxmmer		Y		Y		
rxrcrc		Y	Y	N	N	
rxalgn		Y	Y	N	Y	
rxmacf		Y	N	N		Y (control frame)
rxmacp		Y	N	N		Y (pause frame)
rxbcast		Y	N	N		N (broadcast)

rxmcast	Y	N	N	N (multicast – broadcast)
rxucast	Y	N	N	N (unicast)

rx64 : Receive number of 64 byte packets, including bad packets.  
 rx65127 : Receive number of 65-127 byte packets, including bad packets.  
 rx128255 : Receive number of 128-255 byte packets, including bad packets.  
 rx256511 : Receive number of 256-511 byte packets, including bad packets.  
 rx5121023 : Receive number of 512-1023 byte packets, including bad packets.  
 rx1024max : Receive number of 1024-max size byte packets, including bad packets.  
 rxfler : Receive frame length error

## TX Counters (12)

txbyte: Transmit octet count, good only packets, including pause packets  
 txcrse: Transmit carrier sense error  
 txlcol: Transmit late collision  
 txmacp: Transmit MAC pause frame, full duplex only  
 txbcast: Transmit good broadcast complete  
 txmcast: Transmit good multicast frame count, excluding broadcast frames.  
 txucast: Transmit good unicast  
 txdfr: Transmit defer  
 txtcol: Transmit total collision, half duplex only  
 txscol: Transmit single collision  
 txmcol: Transmit multiple collision  
 txecol: Transmit excessive collision

Memory map for counters for each port:

Port 1	Port 2	Port 3	Port 4
0x00 rxbyte	0x20 rxbyte	0x40 rxbyte	0x60 rxbyte
0x01 rxudsz	0x21 rxudsz	0x41 rxudsz	0x61 rxudsz
0x02 rxfrgm	0x22 rxfrgm	0x42 rxfrgm	0x62 rxfrgm
0x03 rxovsz	0x23 rxovsz	0x43 rxovsz	0x63 rxovsz
0x04 rxjabr	0x24 rxjabr	0x44 rxjabr	0x64 rxjabr
0x05 rxmxer	0x25 rxmxer	0x45 rxmxer	0x65 rxmxer
0x06 rxcrc	0x26 rxcrc	0x46 rxcrc	0x66 rxcrc
0x07 rxalgn	0x27 rxalgn	0x47 rxalgn	0x67 rxalgn
0x08 rxmacf	0x28 rxmacf	0x48 rxmacf	0x68 rxmacf
0x09 rxmacp	0x29 rxmacp	0x49 rxmacp	0x69 rxmacp
0x0a rxbcast	0x2a rxbcast	0x4a rxbcast	0x6a rxbcast
0x0b rxmcast	0x2b rxmcast	0x4b rxmcast	0x6b rxmcast
0x0c rxucast	0x2c rxucast	0x4c rxucast	0x6c rxucast
0x0d rx64	0x2d rx64	0x4d rx64	0x6d rx64
0x0e rx65127	0x2e rx65127	0x4e rx65127	0x6e rx65127
0x0f rx128255	0x2f rx128255	0x4f rx128255	0x6f rx128255
0x10 rx256511	0x30 rx256511	0x50 rx256511	0x70 rx256511
0x11 rx5121023	0x31 rx5121023	0x51 rx5121023	0x71 rx5121023
0x12	0x32	0x52	0x72
rx1024max	rx1024max	rx1024max	rx1024max
0x13 rxfler	0x33 rxfler	0x53 rxfler	0x73 rxfler
0x14 txbyte	0x34 txbyte	0x54 txbyte	0x74 txbyte
0x15 txcrse	0x35 txcrse	0x55 txcrse	0x75 txcrse
0x16 txlcol	0x36 txlcol	0x56 txlcol	0x76 txlcol
0x17 txmacp	0x37 txmacp	0x57 txmacp	0x77 txmacp
0x18 txbcast	0x38 txbcast	0x58 txbcast	0x78 txbcast

0x19 txmcast	0x39 txmcast	0x59 txmcast	0x79 txmcast
0x1a txucast	0x3a txucast	0x5a txucast	0x7a txucast
0x1b txdfr	0x3b txdfr	0x5b txdfr	0x7b txdfr
0x1c txtcol	0x3c txtcol	0x5c txtcol	0x7c txtcol
0x1d txecol	0x3d txecol	0x5d txecol	0x7d txecol
0x1e txscol	0x3e txscol	0x5e txscol	0x7e txscol
0x1f txmcol	0x3f txmcol	0x5f txmcol	0x7f txmcol

Register base counters

0x80 Port 1 txdrop  
0x81 Port 2 txdrop  
0x82 Port 3 txdrop  
0x83 Port 4 txdrop  
0x84 Port 5 txdrop  
0x85 Port 1 rxdrop  
0x86 Port 2 rxdrop  
0x87 Port 3 rxdrop  
0x88 Port 4 rxdrop  
0x89 Port 5 rxdrop

### 3.9.20 LAN PHY Power Management Register for Ports 1 & 2 (LPPM12 Offset 0xE84C)

The following table shows the register bit fields.

BITS	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	0x00	RO	Reserved
25	0	RO	Port 1 MDIXS MDIX Status 1: MDIX 0: MDX
24	0	RO	Reserved
23	1	RW	Port 1 AMDIXP Auto MDIX Parameter 1: follow IEEE specification for auto-negotiation 0: don't follow IEEE specification for auto-negotiation
22	0	RW	Port 1 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
21	0	RW	Reserved
20	0	RW	Port 1 PD Power Down 1: power down 0: normal operation
19	0	RW	Port 1 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
18	0	RW	Port 1 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
	0	RW	Port 1 LPBK Loopback



17			1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
16:10	0x00	RO	Reserved
9	0	RO	Port 2 MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	Reserved
7	1	RW	Port 2 AMDIXP Auto MDIX Parameter 1: follow IEEE specification for auto-negotiation 0: don't follow IEEE specification for auto-negotiation
6	0	RW	Port 2 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	Reserved
4	0	RW	Port 2 PD Power Down 1: power down 0: normal operation
3	0	RW	Port 2 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
2	0	RW	Port 2 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	Port 2 LPBK Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
0	0		Reserved

### 3.9.21 LAN PHY Power Management Register for Ports 3 & 4 (LPPM34 Offset 0xE850)

The following table shows the register bit fields.

BITS	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:26	0x00	RO	Reserved
25	0	RO	Port 3 MDIXS MDIX Status 1: MDIX 0: MDX
24	0	RO	Reserved
23	1	RW	Port 3 AMDIXP Auto MDIX Parameter 1: follow IEEE specification for auto-negotiation 0: don't follow IEEE specification for auto-negotiation
22	0	RW	Port 3 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation

21	0	RW	Reserved
20	0	RW	Port 3 PD Power Down 1: power down 0: normal operation
19	0	RW	Port 3 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
18	0	RW	Port 3 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
17	0	RW	Port 3 LPBK Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
16:10	0x00	RO	Reserved
9	0	RO	Port 4 MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	Reserved
7	1	RW	Port 4 AMDIXP Auto MDIX Parameter 1: follow IEEE specification for auto-negotiation 0: don't follow IEEE specification for auto-negotiation
6	0	RW	Port 4 TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	Reserved
4	0	RW	Port 4 PD Power Down 1: power down 0: normal operation
3	0	RW	Port 4 DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function
2	0	RW	Port 4 FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	Port 4 LPBK Loopback 1: perform "local loopback", i.e. loop back MAC's TX back to RX 0: normal operation
0	0		Reserved

## 3.10 Miscellaneous Registers

### 3.10.1 Device ID Register (DID Offset 0xEA00)

This read-only register holds a 16-bit Device ID.  
The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:16	0	RO	Reserved
15:0	0x8695	RO	Device ID

### 3.10.2 Revision ID Register (RID Offset 0xEA04)

This register holds a 4-bit Revision ID.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:4	0	RO	Reserved
3:0	1	RO	Revision ID

### 3.10.3 WAN Miscellaneous Control Register (WMC Offset 0xEA0C)

This register controls certain additional WAN port features not specified in the WAN DMA registers.

Main features are the in the physical coding sublayer (PCS) functionality.

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31	0	RW	WANPPD WAN Port PHY Power Down When set, the PHY Device of the WAN port is shut down for power saving.
30	0	RO	WANC WAN Auto-Negotiation Complete When set, it indicates the WAN port auto-negotiation has completed.
29	0	RW	WANR WAN Auto-Negotiation Restart Set to restart the WAN port PHY auto-negotiation process.
28	1	RW	WANAP WAN Auto-Negotiation Advertise Pause
27	1	RW	WANA100F WAN Auto-Negotiation Advertise 100 Full Duplex
26	1	RW	WANA100H WAN Auto-Negotiation Advertise 100 Half Duplex
25	1	RW	WANA10F WAN Auto-Negotiation Advertise 10 Full Duplex
24	1	RW	WANA10H WAN Auto-Negotiation Advertise 10 Half Duplex
23	0	RO	WLS WAN Link Status
22	0	RO	WDS WAN Duplex Status (resolved)
21	0	RO	WSS WAN Speed Status (resolved)
20	0	RO	WLPP WAN Link Partner Pause
19	0	RO	WLP100F WAN Link Partner 100 Full Duplex
18	0	RO	WLP100H WAN Link Partner 100 Half Duplex
17	0	RO	WLP10F WAN Link Partner 10 Full Duplex
16	0	RO	WLP10H WAN Link Partner 10 Half Duplex
15	0	RW	WAND WAN Auto-Negotiation Disable
14	0	RW	WANF100 WAN Force 100 when Auto-Negotiation disabled
13	0	RW	WANFF WAN Force Full-Duplex when Auto-Negotiation disabled
12:7	0	RO	Reserved
6:4	0	RW	WLED1S WAN LED1 Select

			000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities
3	0	RO	Reserved
2:0	0x6	RW	WLED0S WAN LED0 Select 000: Speed 001: Link 010: Full Duplex 011: Collision 100: TX/RX Activities 101: Full Duplex/ Collision 110: Link/ Activities

### 3.10.4 WAN PHY Power Management Register (WPPM Offset 0xEA10)

The following table shows the register bit fields.

BIT FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:10	0	RO	Reserved
9	0	RO	MDIXS MDIX Status 1: MDIX 0: MDX
8	0	RO	FEF Far End Fault 1: far end fault status detected 0: no far end fault status detected
7	1	RW	AMDIXP Auto MDIX Parameter 1: follow IEEE specification for auto-negotiation 0: don't follow IEEE specification for auto-negotiation
6	0	RW	TXDIS Disable Port's Transmitter 1: disable port's transmitter 0: normal operation
5	0	RW	DFEF Disable Far End Fault 1: disable far end fault detection & pattern transmission 0: enable far end fault detection & pattern transmission
4	0	RW	PD Power Down 1: power down 0: normal operation
3	0	RW	DMDX Disable Auto MDI/MDIX 1: disable auto MDI/MDIX function 0: enable auto MDI/MDIX function

2	0	RW	FMDX Forced MDIX 1: if auto MDI/MDIX is disabled, force PHY into MDIX mode 0: do not force PHY into MDIX mode
1	0	RW	LPBK Loopback 1: perform “local loopback”, i.e. loop back MAC’s TX back to RX 0: normal operation
0	0	RO	Reserved

### 3.10.5 Test Register 1(WPC Offset 0xEA14)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:24	0	RO	Reserved
23:0	0	RO	Reserved

### 3.10.6 Test Register 2 (WPS Offset 0xEA18)

The following table shows the register bit fields.

BITS FIELD	DEFAULT VALUE	READ/ WRITE	DESCRIPTION
31:8	0	RO	Reserved
7:0	0	RO	Reserved

## 4.0 Host Communication

This chapter describes the descriptor lists and data buffers, which are collectively called the host communication area, that manage the actions and status related to buffer management. Commands and signals that control the functional operation of the KS8695X are also described.

The KS8695X and the driver communicate through the two data structures: System Configuration Registers (SCRs) and Descriptor Lists and Data Buffers.

Note: All unused bits the data structure in this chapter are reserved and should be written by the driver as zero.

### 4.1 Descriptor Lists and Data buffers

The KS8695X transfers received data frames to the receive buffer in host memory and transmits data from the transmit buffers in host memory. Descriptors that reside in the host memory act as pointers to these buffers. There are two descriptor lists, one for receive and one for transmit for each MAC DMA(WAN and LAN). The base address of each list for WAN is written on WTDLB, and WRDLB, respectively. The base address of each list for LAN is written on LTDLB, and LRDLB, respectively. A descriptor list is forward linked. The last descriptor may point back to the first entry to create a ring structure. Descriptors are chained by setting the *next address* to next buffer in both the receive and transmit descriptors.

The descriptor lists reside in the host *physical* memory address space. Each pointer points to one buffer and the second pointer points to the next descriptor. This enables the greatest flexibility for the host to chain data buffers with discontinuous memory location. This eliminates processor-intensive tasks such as memory copying from the host to memory.

A data buffer contains of either an entire frame or part of a frame, but it cannot exceed a single frame. Buffers contain only data; buffer status is maintained in the descriptor. Data chaining refers to frames that span multiple data buffers. Data chaining can be enabled or disabled. Data buffers reside in host physical memory space.

The descriptor structures for WAN and LAR are identical. For simplicity, they are both collectively referred to as RDES0-3, and TDES0-3 for receive and transmit.

## 4.2 Receive Descriptors (RDES0-RDES3)

Receive descriptors and buffers addresses must be Word aligned. Each receive descriptor provides one frame buffer, one byte count field, as well as control and status bits.

The following table shows the RDES0 register bit fields.

BIT FIELD	DESCRIPTION
31	<b>OWN Own Bit</b> When set, indicates that the descriptor is owned by the KS8695. When reset, indicates that the descriptor is owned by the host. The KS8695X clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full.
30	<b>FS First Descriptor</b> When set, indicates that this descriptor contains the first buffer of a frame. If the buffer size of the first buffer is 0, the next buffer contains the beginning of the frame.
29	<b>LS Last Descriptor</b> When set, indicates that the buffer pointed by this descriptor is the last buffer of the frame.
28	<b>IPE IP Checksum Error</b> When set, indicates that the received frame is an IP packet and its IP checksum field does not match. This bit is valid only when last descriptor is set.
27	<b>TCPE TCP Checksum Error</b> When set, indicates that the received frame is an TCP/IP packet and its TCP checksum field does not match. This bit is valid only when last descriptor is set.
26	<b>UDPE UDP Checksum Error</b> When set, indicates that the received frame is an UDP/IP packet and its UDP checksum field does not match. This bit is valid only when last descriptor is set.
25	<b>ES Error Summary</b> Indicates the logical OR of the following RDES0 bits: CRC error Frame too long Runt frame This bit is valid only when last descriptor is set.
24	<b>MF Multicast Frame</b> When set, indicates that this frame has a multicast address. This bit is valid only when last descriptor is set.
23:20	<b>SPN Switch Engine Source Port Number</b> This field indicates the source port where the packet originated. This is valid only for LAN DMA MAC which interconnects with the switch engine. Valid ports range from 0 through 3. This field is valid only when the last descriptor is set. (Bit 23 and 22 is not used, but reserved for backward compatibility and future expansion) Note: To specify receive source port information, transmit pre-tag mode (bit 13 of SEP5C register 0xE818) must be set.
19	<b>RE Report on MII Error</b>

	When set, indicates that a receive error in the physical layer was reported during the frame reception.
18	<b>TL Frame Too Long</b> When set, indicates that the frame length exceeds the maximum size of 1518 bytes. This bit is valid only when last descriptor is set. Note: Frame too long is only a frame length indication and does not cause any frame truncation.
17	<b>RF Runt Frame</b> When set, indicates that this frame was damaged by a collision or premature termination before the collision window has passed. Runt frames are passed on the host only if the pass bad frames bit is set.
16	<b>CE CRC Error</b> When set, indicates that a CRC error occurred on the received frame. This bit is valid only when last descriptor is set.
15	<b>FT Frame Type</b> When set, indicates that the frame is an Ethernet-type frame (frame length field is greater than 1500 bytes). When clear, indicates that the frame is an IEEE 802.3 frame. This bit is not valid for runt frames. This bit is valid only when last descriptor is set.
14:11	Reserved
10:0	<b>FL Frame Length</b> Indicates the length, in bytes, of the received frame, including the CRC. This field is valid only when last descriptor is set and descriptor error is reset.

The following table shows the RDES1 register bit fields.

BIT FIELD	DESCRIPTION
31:26	Reserved
25	<b>RER Receive End of Ring</b> When set, indicates that the descriptor list reached its final descriptor. The KS8695X returns to the base address of the list, thus creating a descriptor ring.
24:12	Reserved
10:0	<b>RBS Receive Buffer Size</b> Indicates the size, in bytes, of the receive data buffer. If the field is 0, the KS8695X ignores this buffer and moves to the next descriptor. The buffer size must be a multiple of 4.

The following table shows the RDES2 register bit fields.

BIT FIELD	DESCRIPTION
31:0	<b>Buffer Address</b> Indicates the physical memory address of the buffer. The buffer address must be Word aligned.

The following table shows the RDES3 register bit fields.

BIT FIELD	DESCRIPTION
31:0	<b>Next Descriptor Address</b> Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.



### 4.3 Transmit Descriptors (TDES0-TDES3)

Transmit descriptors must be Word aligned. Each descriptor provides one frame buffer, one byte count field, as well as control and status bits.

The following table shows the TDES0 register bit fields.

BIT FIELD	DESCRIPTION
31	<p>OWN Own Bit</p> <p>When set, indicates that the descriptor is owned by the KS8695. When cleared, indicates that the descriptor is owned by the host. The KS8695X clears this bit either when it completes the frame transmission or when the buffer allocated in the descriptor is empty.</p> <p>The ownership bit of the first descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between the KS8695X fetching a descriptor and the driver setting an ownership bit.</p>
30:0	Reserved

The following table shows the TDES1 register bit fields.

BIT FIELD	DESCRIPTION
31	<p>IC Interrupt on Completion</p> <p>When set, the KS8695X set transmit interrupt after the present frame has been transmitted. It is valid only when last segment is set.</p>
30	<p>FS First Segment</p> <p>When set, indicates that the buffer contains the first segment of a frame.</p>
29	<p>LS Last Segment</p> <p>When set, indicates that the buffer contains the last segment of a frame.</p>
28	<p>IPCKG IP Checksum Generate</p> <p>When set, the KS8695X will generate correct IP checksum for outgoing frames that contains IP protocol header. The KS8695X supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the IP checksum generate bit in the transmit mode register is not set.</p> <p>This bit should be always set for multiple-segment packets.</p>
27	<p>TCPCKG TCP Checksum Generate</p> <p>When set, the KS8695X will generate correct TCP checksum for outgoing frames that contains IP and TCP protocol header. The KS8695X supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the TCP checksum generate bit in the transmit mode register is not set.</p> <p>This bit should be always set for multiple-segment packets.</p>
26	<p>UDPCCKG UDP Checksum Generate</p> <p>When set, the KS8695X will generate correct UDP checksum for outgoing frames that contains IP and UDP protocol header. The KS8695X supports only standard IP header, i.e. IP with 20 byte header. When this feature is used, ADD CRC bit in the transmit mode register should always be set.</p> <p>This bit is used as a per-packet control when the UDP checksum generate bit in the transmit mode register is not set.</p>
25	<p>TER Transmit End of Ring</p> <p>When set, indicates that the descriptor pointer has reached its final descriptor.</p> <p>The KS8695X returns to the base address of the list, forming a descriptor ring.</p>
24	Reserved
23:20	SPN Switch Engine Destination Port Map

	When set, this field indicates the destination port(s) where the packet will be forwarded to. This field is valid only for LAN DMA MAC which interconnects with the switch engine. Setting all ports to 1 will cause the switch engine to broadcast the packet. Setting all bits to 0 has no effect. The switch engine forwards the packet according to its internal switch lookup algorithm. This field is valid only when the last descriptor is set. Note: To specify destination port on transmit, the Receive direct mode (bit 14 to SEP5C register 0xE818) must be set.
19:11	Reserved
10:0	TBS Transmit Buffer Size Indicates the size, in bytes, of the transmit data buffer. If this field is 0, the KS8695X ignores this buffer and moves to the next descriptor.

The following table shows the TDES2 register bit fields.

<b>BIT FIELD</b>	<b>DESCRIPTION</b>
31:0	Buffer Address Indicates the physical memory address of the buffer. There is no limitation on the transmit buffer address alignment.

The following table shows the TDES3 register bit fields.

<b>BIT FIELD</b>	<b>DESCRIPTION</b>
31:0	Next Descriptor Address Indicates the physical memory address of the next descriptor in the descriptor ring. The buffer address must be Word aligned.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**  
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is a Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2004 Micrel, Incorporated.